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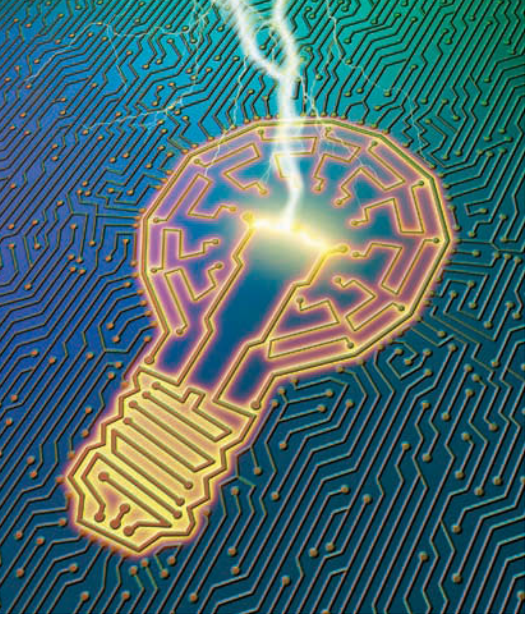

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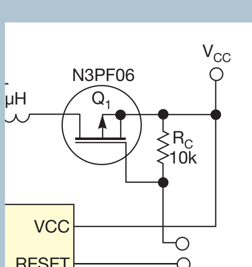

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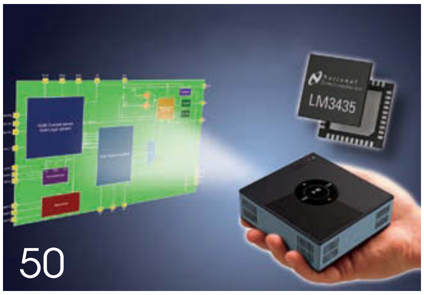

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DEPARTMENTS & COLUMNS

EDN online contents www.edn.com

ONLINE ONLY

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Improved stability of thin-film resistors
Circuit designers often use the time-dependent form of the Arrhenius equation to predict drift in thin-film resistors. Relying on this equation, designers can model resistive-value changes due to aging for any relevant condition in the temperature-time expanse during the resistor's application. In recent years, engineers have used this model in the development of new thin-film resistive layers.
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BY PATRICK MANNION, DIRECTOR OF CONTENT

The spirit in design

About 21 years ago, I'd never even heard of Jim Williams or Bob Pease: I was too busy either looking for work or having a bit more extracurricular fun than I truly deserved. A year later, and 10 months into the trade-publishing business, I knew enough about both of them to handle with kid gloves the two books I got in the mail to review: *Analog Circuit Design*, edited by Jim Williams, and *Troubleshooting Analog Circuits*, by Robert A Pease, both the culmination of series that *EDN* had already published.

Even after only a few months in "the biz," I knew that these two guys were something special, and here, right in my hands, was the physical embodiment of a tiny portion of what they knew or how they thought. I was going to read their books, from cover to cover … after I got my next story out. So, I took them home, put them on my shelf, and got back to work.

Fast-forward 20 years—and many stories later—and those two books were still sitting side by side on a shelf, except the shelf had changed—from an apartment in New York, to an apartment in New Jersey, to a house in New York, and to another house in New York. Besides the shelf, the addition of a wife, two kids, a dog, and a couple of gray hairs, nothing much else had changed: I still was going to read those books, and I was someday going to meet Williams and Pease face to face.

But then, on June 12, everything changed. Williams died of a stroke, and, a bit more than a week later, Pease died at the wheel of his beloved Volkswagen Beetle while leaving a remembrance party for his friend Jim. Although I can't compare what I am feeling to the incredible loss their families and friends feel, shock and sadness still pervade. The bittersweet outpouring of grief and remembrances online across our sites amplifies those feelings (see www.edn.com/110714df2a and www.edn.com/110714df2c).

So here I am, wondering how to say goodbye to two heroes I've never met, meanwhile asking myself how they became so great and who or what will fill the gap they've left behind? I finally reached for those two books, and the answers to the questions became quickly apparent.

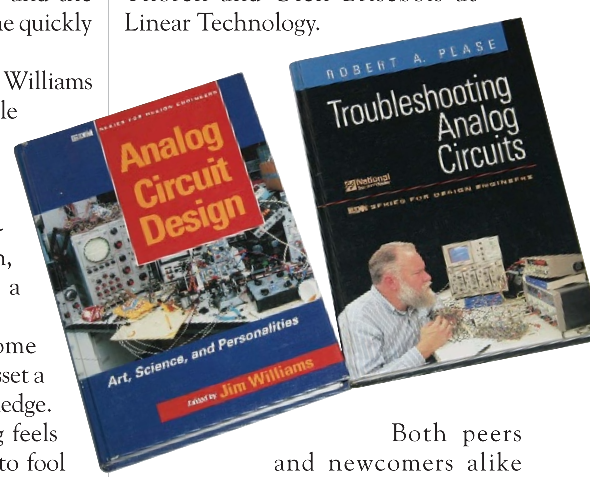
Lacking a formal education, Williams relied upon his own indomitable spirit, curiosity, and love of analog to rise to the top of his profession. Beyond all the formulas, diagrams, laws, and general chaos that is analog design, though, what is it that makes a designer great?

Williams himself gave some pointers: "The single greatest asset a designer can have is self-knowledge. Knowing when your thinking feels right and when you're trying to fool yourself." He added, "Knowing your strengths and weaknesses, prowesses and prejudices. Learning when to ask questions and when to believe your answers."

Besides the passion for electronics and hands-on learning, both Williams and Pease had another quality: humility, along with a recognition that they owed those who came before them. Both acknowledged the many contributions of op-amp pioneer George Philbrick to their personal and career development, and Pease paid special homage in his book to the late Bruce Seddon, an engineer who helped him "appreciate the niceties of worst-case design." Seddon always lent his ear and helping hand. Wrote Pease, "And if I never got around to saying thank you—well, 30 years is a long time to be an ungrateful, lazy bum, but now's the time to say, 'Thank you, Bruce.'"

Pease took the example of Seddon to heart and practiced the same principles, day in and day out, as did Williams in his own way. It's with that example in mind that I acknowledge the futility of looking for other heroes to fill the space they leave behind or of the need to say goodbye.

Many heroes are out there today, from the ones we know—Barrie Gilbert, Bonnie Baker, Howard Johnson, Dan Sheingold, Walt Jung, and Walt Kester—to the up-and-comers *EDN*'s Paul Rako points to: Bob Thomas at Cisco, Francis Lau at Tyco/Elo Touch, Eric Schlaepfer at Maxim, and Mark Thoren and Glen Brisebois at Linear Technology.



Both peers and newcomers alike are wiser and better for having had the gift of Williams and Pease. They have not left us; their spirits live throughout the community in everyone they've touched and helped, and in every electronic device we hold and use. So, there is no need to say goodbye; just a simple thank-you is enough. EDN

Contact me at patrick.mannion@ubm.com.

Peak-power analyzer boasts accuracy, fast rise and fall times

Agilent has announced the 8990B peak-power analyzer, which, according to the company, offers the highest measurement speed and greatest measurement accuracy in pulse-peak-power analysis for aerospace, defense, and wireless applications. The N1923A and N1924A wideband power sensors complement the 8990B. The N1923A and N1924A cover frequency ranges of 50 MHz to 18 GHz and 50 MHz to 40 GHz, respectively. With either sensor, the 8990B achieves 5-nsec rise/fall times—according to Agilent, the shortest overall rise/fall times among all such instruments—for measuring and analyzing RF pulses.

Offering ease of use and high performance, the 8990B comes with a 15-in.-diagonal, 1024×768-pixel XGA (extended-graphics array) color touchscreen that simultaneously displays four-channel results for maximum image detail. With its acquisition rate of 100M samples/sec, the instrument provides the high speed and resolution that R&D engineers need to detect, explain, and eliminate signal anomalies.

The 8990B makes 15 predefined pulse-parameter measurements, including rise time, pulse droop, pulse width, and time delay. You can automatically measure these parameters in two easy steps using the touchscreen. These parameter measurements are key elements of the design, testing, and validation of power amplifiers, transmitter/receiver modules, transponders, radar-test sets, satellite payloads, and other devices that require careful control of complex aspects of their performance.

US price for the 8990B peak-power analyzer is $28,500. US prices for the N1923A and N1924A wideband power sensors begin at $5000.—**by Dan Strassberg**

▷**Agilent Technologies**, www.agilent.com/find/peakpoweranalyzer.

With either of its two state-of-the-art wideband power sensors, the 8990B peak-power analyzer makes possible accurate measurements of RF pulse parameters in aerospace, defense, and wireless applications.

TALKBACK

"One day I backed into the dc-contactor box with a 12-inch screwdriver in my back pocket. The screwdriver melted, and it didn't even phase the dc-contactor box at all. That was the last time I didn't remember to remove everything from my pockets."

—retired electronics technician John W Lynch, in *EDN*'s Talkback section, at http://bit.ly/moEPmM. Add your comments.

12-bit scopes take 2G samples/sec, provide extensive waveform analysis

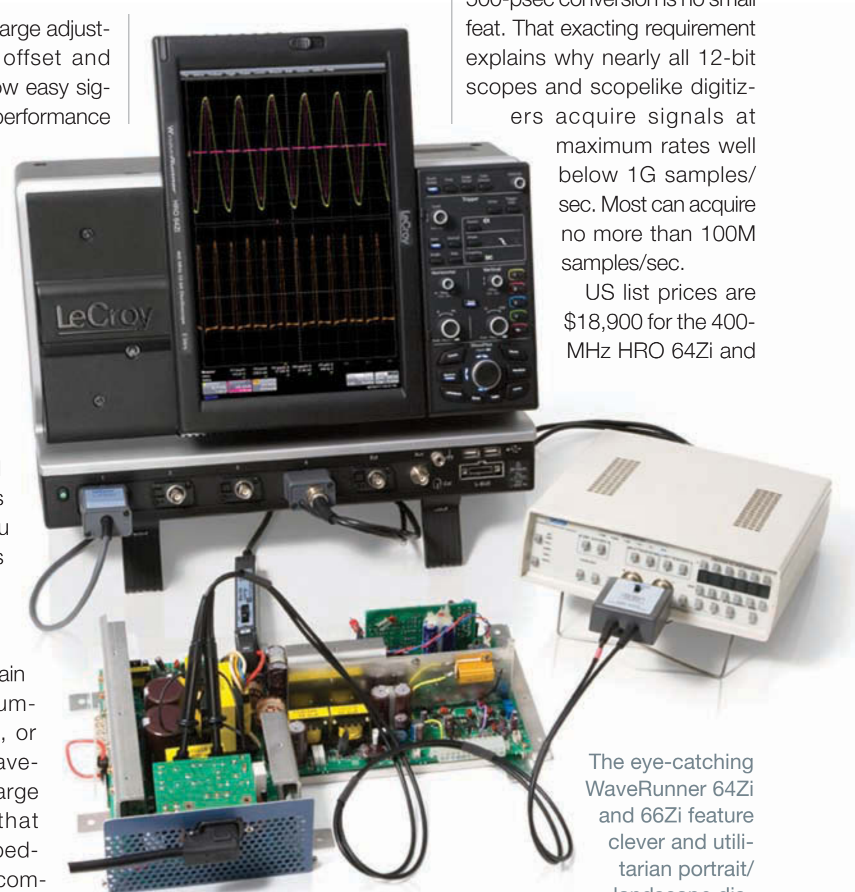
LeCroy has introduced a line of 12-bit-resolution, four-channel, 400- and 600-MHz-bandwidth WaveRunner 6 Zi HROs (high-resolution oscilloscopes), which feature 2G-sample/sec, 12-bit ADCs, memory as deep as 256M points/channel on all channels, and superior dc accuracy. These features combine with WaveRunner 6 Zi series' extensive analysis capabilities, so you no longer must sacrifice oscilloscope-grade analysis to capture 12-bit data at rates to several billion samples/sec.

Targeting use in medical, automotive, power, and electromechanical applications, the HROs provide higher resolution and greater measurement precision than do traditional 8-bit alternatives, which are often inadequate for viewing signals with both large and small voltage components. The 12-bit architecture yields ±0.5% dc-gain accuracy and 55-dB SNR (signal-to-noise ratio)—almost eight times typical 8-bit scopes' 38 dB.

The 256M-point/channel waveform memory enables the capture of 28.6-sec records on each channel at 10M samples/sec and, at higher sampling rates, the capture of shorter records with time resolution as fine as 500 psec. Large adjustment ranges for offset and timebase delay allow easy signal- and amplifier-performance assessment and enable zooming in on vertical and horizontal signal features. The HROs also provide a pivoting display that permits viewing signals in portrait or landscape modes to obtain more detail for analysis. This feature allows you to view as many as 36 channels using the mixed-signal option, operate in the frequency domain using the spectrum-analysis package, or view decoded waveforms using the large selection tools that focus on the embedded-system and communications markets.

Some scopes with 8-bit ADCs offer enhanced resolution through the use of techniques such as averaging of large numbers of nominally identical waveforms, reducing noise by passing the signal through extremely narrowband-DSP-based filters, or counter-intuitively by adding dither to the waveform you are measuring. However, those techniques, which require users to thoroughly understand the enhancement approach, suffer from limitations that do not apply to systems employing high-resolution ADCs. On the other hand, 12-bit conversions require an ADC to resolve 4096 voltage levels. Resolving such small voltage differences in a 500-psec conversion is no small feat. That exacting requirement explains why nearly all 12-bit scopes and scopelike digitizers acquire signals at maximum rates well below 1G samples/sec. Most can acquire no more than 100M samples/sec.

US list prices are $18,900 for the 400-MHz HRO 64Zi and $22,900 for the 600-MHz HRO 66Zi. The standard versions of both units provide waveform-memory depth of 64M samples/channel on all four channels independent of the number of channels in use. An increase to 128M samples on each channel adds $6500 to the base price, and an increase to 256M samples adds $8500.



The eye-catching WaveRunner 64Zi and 66Zi feature clever and utilitarian portrait/landscape displays and combine a 12-bit-resolution, 2G-sample/second ADC on each of their four channels with a complement of built-in scope-level signal-analysis features.

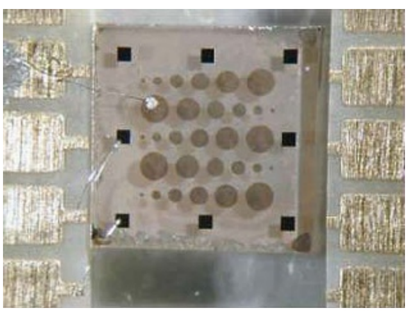
—by Dan Strassberg

▷**LeCroy Corp**, www.lecroy.com/oscilloscope/oscilloscopeseries.aspx?mseries=352.

DILBERT By Scott Adams

Physical phenomenon could lead to clock-speed increases

Researchers at the Massachusetts Institute of Technology and at the University of Augsburg have discovered a new physical phenomenon that could yield transistors with greatly enhanced capacitance, which, in turn, could lead to the revival of clock speed as the measure of a computer's power (**Reference 1**). The research focuses largely on lanthanum aluminate, which comprises alternating layers of lanthanum oxide and aluminum oxide. The lanthanum-based layers have a slight positive charge; the aluminum-based layers, a slight negative charge, according to the MIT researchers. The result is a series of electric fields that all add up in the same direction, creating an electric potential between the top and the bottom of the material.



The researchers' experimental setup comprised a sample of the lanthanum-strontium titanate composite, which looks like a slab of thick glass, with thin electrodes deposited on top of it (courtesy Ashoori Group).

Physicists usually consider both lanthanum aluminate and strontium titanate to be excellent insulators in that they conduct no electrical current. They speculate, however, that, if the lanthanum aluminate were thick enough, its electrical potential would increase to the point that some electrons would have to move from the top of the material to the bottom to prevent a "polarization catastrophe." The result is a conductive channel at the juncture with the strontium titanate, much like the one that forms when you switch on a transistor.

The researchers measured the capacitance between that channel and a gate electrode on the lanthanum aluminate. Admitting that using experimental apparatus somewhat limited their results, the researchers said that an infinitesimal change in voltage causes a large charge to enter the channel between the two materials. "The channel may suck in charge … like a vacuum, and it operates at room temperature, which … really stunned us," says Raymond Ashoori, a professor of physics at MIT.

The material's capacitance is so high that physics cannot explain it. "We've seen the same kind of thing in semiconductors, but that [phenomenon] was a very pure sample, and the effect was very small," says Ashoori. "This [sample] is superdirty and [has] a superbig effect. It could be a new quantum-mechanical effect or some unknown physics of the material."

According to Jean-Marc Triscone, a professor of physics at the University of Geneva, whose group has published several papers on the juncture between lanthanum aluminate and strontium titanate, the computer industry and physics textbooks have long used—and assumed correct—a formula for capacitance. The MIT and University of Augsburg researchers showed that it is now necessary to modify that formula to describe their system.

Although a lot of charge moves into the channel between materials with a slight change in voltage, it moves too slowly for the type of high-frequency switching that takes place in computer chips. Purer samples might exhibit less electrical resistance. If researchers can understand the physical phenomena underlying the material's remarkable capacitance, however, they may be able to reproduce them in more practical materials. "It's not going to revolutionize electronics tomorrow, but this mechanism exists, and, once we know it exists, if we can understand what it is, we can try to engineer it," says Ashoori. Ashoori worked with Lu Li, a postdoctoral and Pappalardo Fellow in his MIT lab, together with Christoph Richter, Stefan Paetel, Thilo Kopp, and Jochen Mannhart of the University of Augsburg.

—**by Suzanne Deffree**

▷**Massachusetts Institute of Technology**, www.mit.edu.

▷**University of Augsburg**, www.uni-augsburg.de/en.

REFERENCE

1 Li, Lu; Christoph Richter; Stefan Paetel; Thilo Kopp; Jochen Mannhart; and Raymond C Ashoori, "Very Large Capacitance Enhancement in a Two-Dimensional Electron System," *Science*, Volume 332, No. 6031, May 13, 2011, pg 825, http://bit.ly/iuty13.

07.14.11

TOOL NOW SUPPORTS OPTIMIZED SPICE ENGINE, MULTICORE PROCESSORS

Texas Instruments has improved its Tina-TI Spice tool, which is available in English, simplified and traditional Chinese, Japanese, and Russian. Tina-TI 9.1 now supports multicore processors and an optimized Spice engine, enabling it to run simulations an average of five times faster than previous versions. It allows designers to import any Spice model to simulate designs and features more than 500 part models and reference designs, including more than 130 new power models. The broad model coverage and fast simulation in Tina-TI 9.1 make it easier for designers to speed their products to market.

Tina-TI 9.1 provides all of the conventional dc, transient, and frequency-domain analysis of Spice and extensive postprocessing capability that allows users to customize results. Virtual instruments allow users to select input waveforms and probe circuits' node voltages and waveforms.

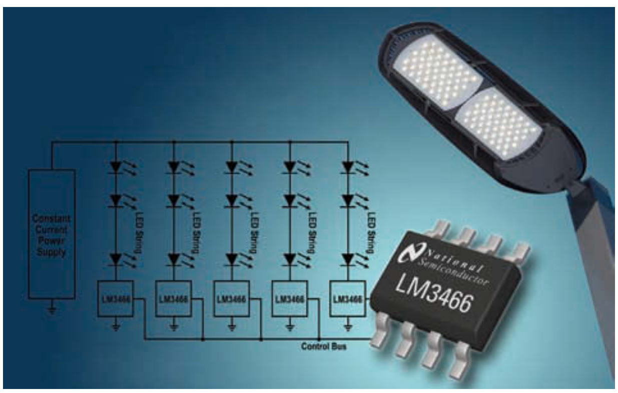
Tina-TI 9.1 is available for free downloading in the TI Analog eLab Design Center at www.ti.com/analogelab-pr.

—by Paul Rako

▸**Texas Instruments**, www.ti.com.

Current driver targets LED strings in streetlights

Lighting fixtures that cover wide areas, such as streetlights, often use LED matrices comprising strings of HB LEDs (high-brightness light-emitting diodes) that rely on off-the-shelf constant-current, ac/dc power supplies. Because the ac/dc power supply drives the entire matrix, complications can arise when one string fails open or begins to draw too much current. These situations can overstress the string's LEDs and create either a gap or a noticeable bright streak in the matrix. However, providing current control for each string adds too many components and increases the light's cost.



The linear LED-driver LM3466 guards against string failures in LED matrices in wide-area lighting.

To address these problems, National Semiconductor has introduced the LM3466 linear LED driver, which integrates a 70V, 1.5A N-channel MOSFET and a linear-control approach, allowing one LM3466 along with one resistor and one capacitor to drive a string of LEDs. Paralleling any number of strings results in a complete LED matrix.

The chip's dynamic-current-equalizing-control scheme enables communication between each LM3466 LED driver to divide current equally or ratiometrically among multiple active LED strings. During an open-string state, each LM3466 automatically equalizes current throughout remaining strings to maintain relatively constant output power.

Each LM3466 conducts a current as high as 1.5A and accepts an input range of 6 to 70V. The LM3466 includes a fault-status output and input-undervoltage-lockout, current-limit, and thermal-shutdown protection.

Linear circuitry prevents any EMI (electromagnetic interference) and ensures compliance with EMC (electromagnetic-compatibility) regulatory requirements. The device requires neither communication with the constant-current power supply nor LED voltage binning. The LM3466 LED driver comes in an eight-pin ePSOP package and sells for $1.30 (1000).

—by Margery Conner

▷**National Semiconductor**, www.national.com.

CST adds HPC, eigenmode-solver support

Engineers are increasingly looking for ways to speed up complex simulations and turning to various HPC (high-performance-computing) techniques, such as multicore processors, server farms, and GPUs (graphics-processing units). Although electromagnetic simulation can reduce the number of prototyping cycles, the increase in simulation-model size still represents a special challenge, according to Martin Timm, marketing director at CST (Computer Simulation Technology). To address that challenge, CST supports HPC techniques to help its customers deal with the trend in microwave- and RF-device design toward increasing device complexity and an accompanying decrease in time for R&D.

The new CST simulation-acceleration scheme provides customers with a choice of HPC features. The CST Microwave Studio 2011 transient solver, for example, now supports Nvidia (www.nvidia.com) Tesla 20 series to provide increased performance with minimal investment. For large or complex models, CST recommends cluster computing. To support communication among nodes in such environments, CST now offers an MPI (message-passing interface) that supports the InfiniBand high-throughput, low-latency interconnection to help ensure scalability. MPI-based parallelization is now available for the integral equation solver, implementing the MLFMM (multilevel fast-multipole method) in Microwave Studio 2011.

CST Studio Suite 2011 also now comes with a simple job-queuing system, and designers can easily integrate it with free or commercial systems, such as the LSF (load-sharing facility) from Platform Computing (www.platform.com) or the OGE (Oracle Grid Engine) from Oracle (www.oracle.com/us).

CST also announced a new finite-element-based eigenmode solver in CST Microwave Studio 2011. The computation of eigenmodes in simulations helps determine parameters such as resonance frequencies and Q values for resonant structures, such as cavities, filters, and particle accelerators. An additional application of eigenmode solvers is the design of periodic devices, such as slow-wave structures, including traveling-wave tubes, and metamaterials, from which engineers can derive phase diagrams from unit cells.

> “The techniques help customers deal with the trend in device design toward increasing complexity.

The new HPC and eigenmode-solver functionalities are available with CST Microwave Studio 2011 Service Pack 3. It is now available for downloading for customers with valid maintenance contracts for the respective options.

—by Rick Nelson

▷**CST**, www.cst.com.

BY PALLAB CHATTERJEE, CONTRIBUTING TECHNICAL EDITOR

Nanomaterials for energy storage

The increasing demand for mobile devices, solar cells, and electric vehicles brings up one fundamental question: How long and how efficiently can they operate before they run out of power? The functional period of both mobile devices and electric vehicles depends on how long the battery will last per charge, how long it takes to charge them up again, and how many times a user can charge them. Solar cells depend on the amount of light necessary to produce electricity from them and how efficiently the energy converts into electricity that can pass on to the device. None of these issues has seen much progress in the past 100 years or so. With the help of new nanomaterials, however, things have recently begun to change.

For example, Nanotecture (www.nanotecture.co.uk) has developed several new nanoporous production processes that allow for materials with high surface areas, which can improve the performance of batteries. One of their first applications is the creation of a hybrid supercapacitor. This product features one carbon electrode with a nickel-hydride nanoporous battery electrode. The approach allows for the increased efficiency and deep power storage of a battery and provides for the reduced discharge and leakage of a capacitor.

Supercapacitors are becoming key components in most mobile systems due to their ability to hold high levels of constant voltage under low current drains for system configuration and nonvolatile-memory support in mobile systems. Supercapacitors have long found use in electronic-flash, mobile-phone, and FPGA-system applications. Current lithium-ion supercapacitors have an in-use life of approximately three years; the new, lower-cost nickel-hydride technology significantly improves that lifetime (**Figure 1**).

These materials go beyond the handheld-mobile-system market to address the energy community, including automotive applications. The product aims to replace standard lead-acid batteries in trucks with the lighter and more powerful supercapacitors. The cost- and weight-sensitive automotive market will benefit from chemical processing for the creation of the nanoporous electrodes—a major breakthrough in this technology.

The use of nanomaterials also has a big impact on photovoltaic and solar products. The increased surface of these materials can react with photons in a solar cell, increasing the net electrical power the cell generates. The new technologies from Nanotecture, other processing methods for nanoporous material creation, and the use of nanowires are all major areas of development for improving solar cells. The key is to find an inexpensive high-volume-manufacturing process that will produce more-than-50%-efficient cell-power conversion. Current solar-cell efficiency ranges from 10 to 19%, and some cells are as low as 1 to 9% efficient.

The nanomaterial work for solar comprises applications of quantum dots; insertion of new materials, including organic and inorganic nanoparticle materials, into the solar-cell structure; new nanodeposition techniques for creating 3-D materials; and nanowire technologies. Universities and commercial facilities are performing this work.

In addition to the discharge-rate and depth problems, batteries also have issues with charging times. For typical short-period use, such as in an electric vehicle driving fewer than 100 miles, which can be measured in minutes, it takes hours to charge the batteries. Researchers at the University of Illinois—Urbana-Champaign recently published a paper describing a method that reduces the energy-capacity loss for batteries when they use fast charge and discharge rates. This method results in a lithium-ion battery that requires only two minutes to provide a 90% charge level. The approach involves cathodes that the researchers created from a 3-D nanostructure. EDN

Pallab Chatterjee is on the IEEE Nanotechnology Council.

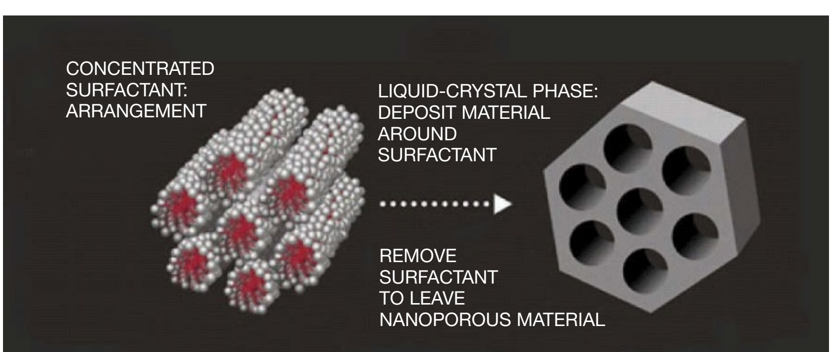


Figure 1 A new, lower-cost nickel-hydride technology significantly improves supercapacitor lifetime (courtesy Nanotecture).

TRACKING PLL DESIGN THROUGH THE DECADES

THE VENERABLE PLL IS VITAL TO TODAY'S IC DESIGN.

BY JEFF GALLOWAY AND ANDREW COLE • SILICON CREATIONS

PLLs (phase-locked loops) are among the most common types of analog/mixed-signal circuits on today's SOC (system-on-chip) ICs. PLLs are essential companions to the digital-logic circuits and processors on these chips. Today's SOCs are likely to integrate many types of PLLs. Like the digital circuits on these SOCs, the continual advances in process technology benefit analog/mixed-signal circuits. Clever designers have made many contributions that have increased the performance of analog/mixed-signal circuits, and PLLs in particular, beyond what you would expect from simple scaling.

The advances in process technology and circuit techniques have allowed PLLs to become smaller and consume far less power per megahertz of output frequency and to achieve better performance than that of PLLs of decades past. The advances have made possible applications for PLLs, including SERDES (serializer/deserializer) circuits and RF integration.

A BIT OF HISTORY

PLLs date back to the 1920s, but their popularity and applications took off with the introduction of the monolithic PLL. The 4046 CMOS Micropower PLL, which RCA (www.rca.com) introduced in the 1970s, is one of the early PLL ICs. These ICs found use in many applications, including frequency synthesis, FM demodulation and modulation, voltage-to-frequency conversion, and data synchronization. The 4046 integrated two types of phase detectors—a linear mixer and an edge-triggered phase/frequency detector—with a VCO (voltage-controlled oscillator) and an output buffer that allowed designers to use the tuning voltage for demodula-

IMAGE: THINKSTOCK

AT A GLANCE

- PLLs (phase-locked loops) date back to the 1920s.
- Monolithic PLLs opened new horizons.
- Good on-chip inductors enabled new levels of PLL performance.
- PLLs now serve a range of applications, and an SOC (system on chip) may have 20 of them.

tion applications. By adding an external divider, you could configure the circuit as a frequency synthesizer, with a range from tens of kilohertz to slightly more than 1 MHz and a power dissipation of tens of microwatts to 1 mW. Designers had to add an external loop filter, but that requirement provided flexibility in setting the loop dynamics.

Fast-forward to today. The most common type of PLL for SOC applications is the frequency-multiplying PLL. This type of PLL generates a high-frequency clock from a low-frequency crystal or another reference. Applications for frequency-multiplying PLLs are widespread and include logic clocking and RF local-oscillator synthesis. It is common for a modern SOC to contain five to 10 of these PLLs.

It is interesting to compare a modern SOC multiplying PLL with one using the 4046 chip, an external feedback divider, and the external loop-filter components (**Figure 1**). The 4046-based circuit would consume several hundred square millimeters of PCB (printed-circuit-board) area, whereas this SOC PLL has an area of approximately 0.07 mm^2—roughly 2000 times smaller. These fully integrated PLLs also include more features. The typical output frequency is 2 GHz, or about 2000 times larger, and the power dissipation is similar. The modern circuit also offers power consumption that is approximately 2000-times better in terms of watts per megahertz.

Most of the advances in frequency, power per megahertz, and area are due simply to advances in process technology and would not be surprising to anyone familiar with Moore's Law. The SOC PLL in **Figure 1** integrates more than 25,000 transistors, whereas the 4046 chip used roughly 5.6 mm^2 for its 150 components (**Reference 1**). The ability to integrate many more transistors has enabled analog/mixed-signal-circuit designers to exercise their creativity and increase their designs' performance.

ADVANCES IN RESOLUTION

Most frequency-synthesis PLLs incorporate a predivider (÷N) and postdividers (÷P), plus a feedback divider (÷M), generating a frequency of F_{IN}×M/(N×P). The resolution in output frequency is F_{IN}/(N×P). Making these dividers larger yields finer resolution. However, this improvement comes at a cost in other important performance parameters.

As N increases, the PLL comparison frequency decreases, and PLL bandwidth must decrease proportionally. A decrease in bandwidth increases the lock time and PLL area—because the loop filter must grow—and the long-term jitter gets worse. Increasing P requires the VCO to run P times faster. A P value of two to four is common for many applications. For large P values, however, the required VCO frequency could exceed the process limitations. Additionally, the power in the VCO and dividers scales with the VCO frequency. So, using the postdivider to achieve fine frequency resolution has serious drawbacks, as well. One way to avoid these trade-offs is to use a noninteger divide value for one of the dividers; fractional-N PLLs employ this approach.

You can achieve a fractional divider value of, for example, 10.25 by the following set of divider values: 10, 10, 10, 11, 10, 10, 10, 11, and so on. You can implement such a variable-ratio divider with a simple accumulator (**Figure 2** and **Reference 2**). Next, you must decide which of the three dividers should be fractional. The first choice—the postdivider—has the problem of transferring the noise or jitter of the divider modulation directly to the output—usually, an unacceptable situation. Assuming that the PLL holds the VCO frequency steady, the output period would vary by a whole VCO period. To minimize jitter, the VCO would need a small period, corresponding to a high frequency.

The predivider and postdivider are better choices for modulation because, in these configurations, the PLL acts as a lowpass filter on the noise or jitter

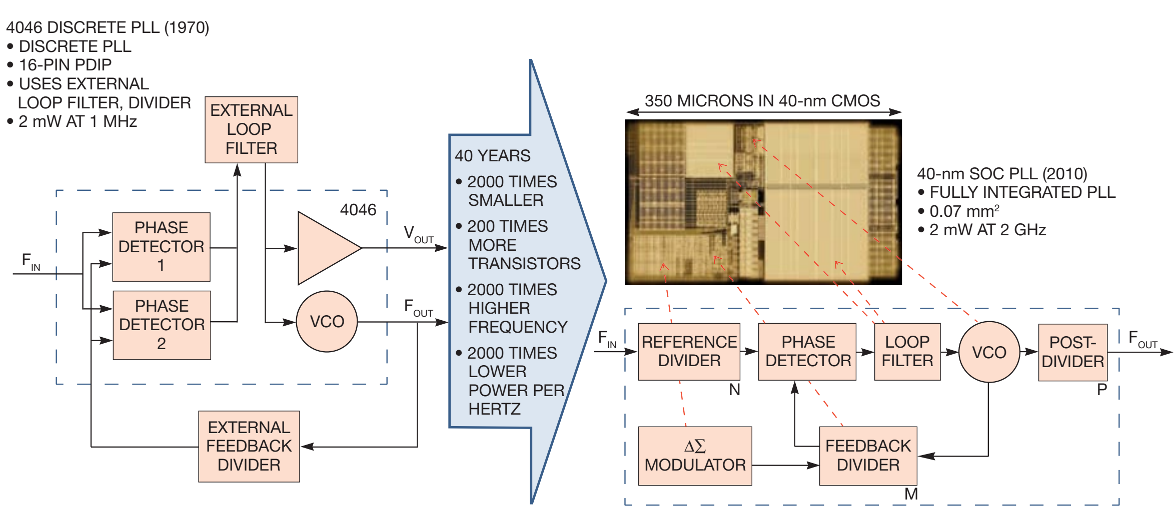


Figure 1 Comparing a 1970s PLL (left) to a recent one (right) illustrates the progress that has occurred over the decades.

associated with modulating the feedback divider. The following **equation** relates the VCO frequency and the reference frequency: $F_{VCO}=F_{REF}\times M/N$. For most practical PLLs, the value of M is larger than that of N, meaning that the VCO period is smaller than the reference period. So, dithering the feedback divider has a smaller effect than dithering the reference divider by the ratio of M/N, making this choice the most common one. Circuits of this type, using multiple ICs, began to appear in the late 1970s and early 1980s.

In the example of the sequence for generating a divider value of 10.25, the divide pattern repeats every four cycles. This approach generates a noise tone at $F_{REF}/4$. If you use the same method to generate an effective value of 10.01, then a tone would appear at $F_{REF}/100$. The spectral tone is problematic for many systems that would like to take advantage of the fine frequency resolution that fractional-N PLLs provide. If this noise tone falls to a frequency below the PLL's bandwidth, considerable long-term jitter, unacceptable in many applications, can result.

A breakthrough in the evolution of the fractional-N PLL was the application in 1993 of delta-sigma modulation to the dithering of the feedback divider (**Figure 2** and **Reference 3**). The delta-sigma-modulation noise-shaping technique can push dithering noise to high frequencies, at which the PLL can easily filter it. Using this technique, designers have created PLLs with nearly undetectable fractional spur tones. Integrated fractional-N PLLs still fall short of the performance of similar integer-N PLLs, however, because of the low bandwidth necessary to filter the dithering noise. With lower bandwidth, the PLL is less able to suppress the phase noise of the VCO.

The dithering noise from the delta-sigma modulator is a pseudorandom pattern. A recent refinement in integrated PLLs cancels this noise by applying a correction directly to the loop filter. Industry literature reports improvements of 10 to 20 dB, allowing designers to increase the bandwidth of fractional-N PLLs, with benefits in circuit area, phase noise, and jitter. In this way, the performance of fractional-N PLLs can approach that of integer-N PLLs. The SOC PLL in **Figure 1** takes advantage of Moore's Law to integrate a 24-bit modulator, allowing the output-frequency increment to be 0.06 ppm or smaller—an extremely fine resolution.

ADVANCES IN PLL QUALITY

Beginning in the early '90s, IC designers began to incorporate passive inductors into ICs fabricated in generic CMOS-logic processes (**Reference 4**). The inductors have lower Q (quality) factors than do discrete components or similar

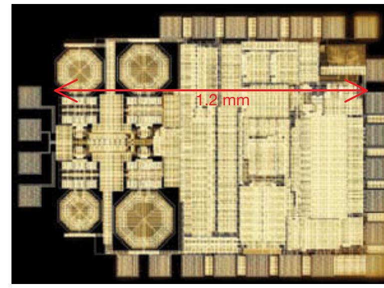


Figure 3 Integrated inductors have changed the appearance and performance of monolithic PLLs.

inductors in an IC process tailored for RF. For decades, ICs have included capacitors in many forms, including gate-oxide, polysilicon-to-polysilicon, and metal-to-metal devices. The use of integrated inductors along with capacitors to form completely integrated LC (inductor/capacitor) VCOs greatly boosts performance (**Figure 3**). For a given fixed power level, LC VCOs typically outperform ring oscillators by 20 dB.

The LC-oscillator circuit predates IC technology. However, the integration of LC oscillators had been problematic until only the last 10 to 15 years. The first problem had to do with the inductor itself. In process nodes larger than 0.25 microns, it was uncommon to have more than three metal layers, and the typical interconnect metal was aluminum. Inductors in this process

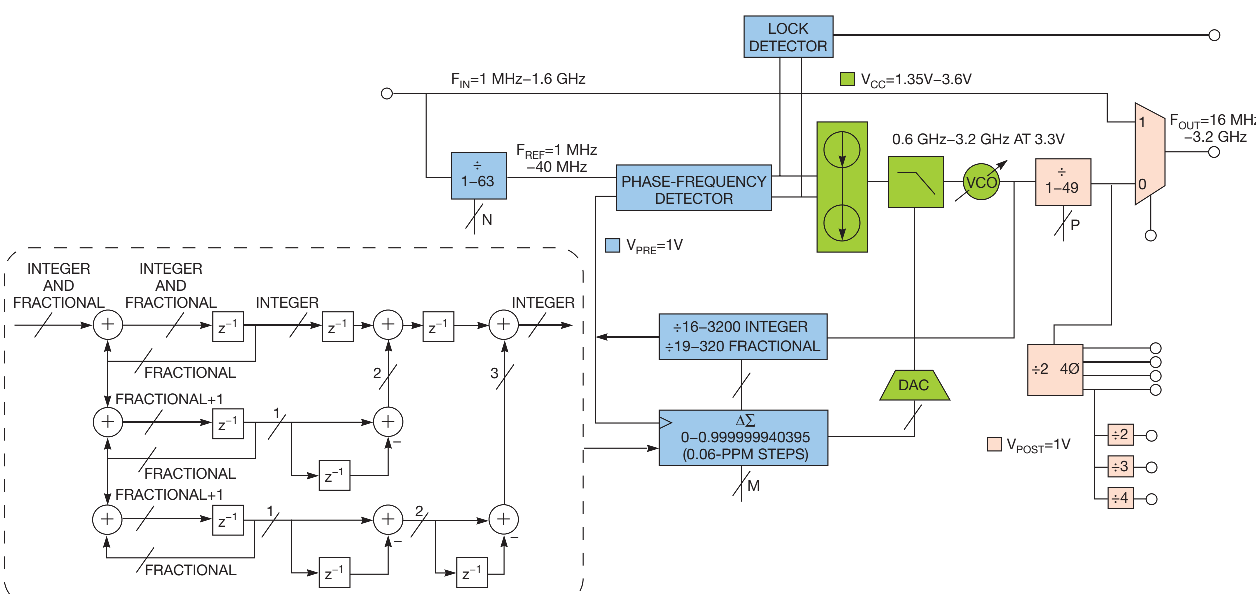


Figure 2 The fractional-N divider and delta-sigma modulator represent relatively recent design advances.

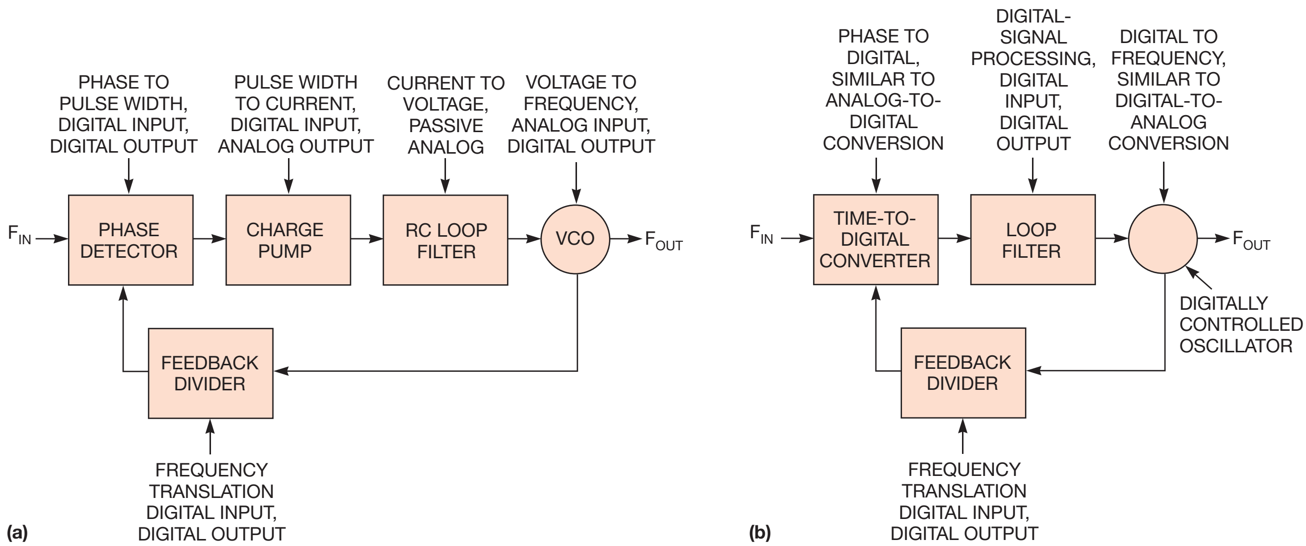


Figure 4 Analog PLLs (a) may be significantly larger than their digital counterparts (b).

had relatively high series resistance, resulting in a low Q factor. The limited number of metal layers also meant that the inductor was physically close to the silicon surface. This situation in turn meant that these inductors had significant parasitic capacitance and hence a low self-resonant frequency.

The desire to integrate more gates has driven two advances in CMOS-processing technology, enabling the integration of practical inductors in generic CMOS-logic processes. The first, the use of CMP (chemical-mechanical polishing), makes each layer in the interconnect stack more planar, allowing for many stacked metal layers. In 180-nm technology, which debuted in the late 1990s, the use of six metal layers became common. Recent process technologies at 65 nm and smaller allow for 10 or more metal layers. The increase in metal layers allows designers to put the inductors in the top metal layers, far above the silicon surface, reducing the parasitic capacitance and increasing the self-resonant frequency. The second advance, the use of copper interconnect, allows for lower series resistance and a higher Q factor because copper interconnect has a lower resistance than aluminum.

The next problem related to the integration of inductors involved the relationship between inductance, oscillation frequency, and tank impedance: $\sqrt{(L/C)}$. The oscillation frequency is proportional to $1/\sqrt{(L \times C)}$. If capacitance is constant, a 2-GHz oscillator requires an inductor that is only 25% the size of a 1-GHz oscillator. As CMOS technologies have advanced, higher frequencies have become possible, allowing smaller inductors. Hence, it has become economical to design and manufacture ICs with on-die inductors.

The performance of LC oscillators in integrated PLLs allows designers to choose integrated PLLs for applications with demanding phase noise, such as SONET (synchronous-optical-network) data transmission and cellular communication, which often require less than 1 psec of long-term jitter. Other advances in circuit design and process technology have allowed the integration of entire RF transceivers.

CURRENT, FUTURE WORK

A current area of interest in PLLs is the digital PLL. Digital PLLs have a digital loop filter rather than an analog loop filter. The biggest advantage of a digital loop filter over an analog loop filter is size (**Figure 4**). For analog PLLs, the size of the loop filter is a strong function of the PLL's bandwidth. For high-bandwidth PLLs, the loop filter consumes approximately 50% of the PLL area. For low-bandwidth PLLs, the loop filter can become a large percentage of the PLL area. Even worse, a low-bandwidth analog PLL may require an external loop filter consuming valuable I/O pins and PCB area. In contrast, as process technology advances, the area taken by adders and registers of a digital loop filter becomes steadily less important.

In digital PLL, these designs require perhaps

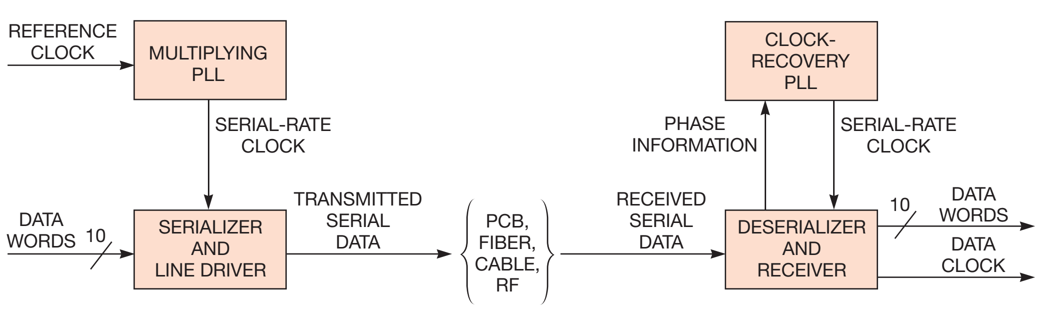


Figure 5 Serial chip-to-chip links have become important applications of PLLs.

as much analog design as would a PLL using an analog loop filter. The analog PLL has two main analog design tasks. The charge pump and loop filter first convert PWM signals from the digital phase detector to current pulses and, in turn, to an analog control voltage. The VCO then produces a frequency proportional to the analog tuning voltage.

The digital PLL replaces the digital phase detector of the analog loop by a phase-to-digital converter or time-to-digital converter. Think of this block as a sort of ADC but with an analog quantity that is phase or time rather than voltage. A DCO (digitally controlled oscillator) then replaces the VCO in the analog loop. This circuit is a type of DAC in which the analog quantity is frequency rather than voltage. So digital-PLL design still has many challenging analog aspects.

Besides an area advantage, the digital loop filter also enjoys a noise advantage when scaling. The voltage noise on the analog loop filter scales as $\sqrt{(kT/C)}$, where k is the Boltzmann's constant, T is the absolute temperature, and C is the loop filter's capacitance. If a design requires the noise to be a factor of two lower, capacitance must increase by four times. With the digital loop filter, the quantization noise scales as 0.5^N, where N is the number of bits. To reduce the noise by a factor of two, a designer needs to add only a bit. A designer can easily make the quantization noise in the digital loop filter negligible for little cost in area. However, this action pushes the problem of noise onto the time-to-digital converter and the DCO. Designing a time-to-digital converter and a DCO with a large number of effective bits is still a significant challenge.

USES FOR SMALLER PLLs

Advances in both circuit design and process technology have allowed SOCs to integrate more PLLs of various types. Besides frequency synthesis, several other applications of PLLs have become important. The integration of PLLs forms one of the keys to serial chip-to-chip communication. This type of communication requires a SERDES circuit pair. Serial chip-to-chip communication has many benefits, most notably the reduction in IC area, because the PLL and SERDES are typically smaller than the set of parallel I/Os, and in PCB complexity because the serial links require fewer traces. The last decade has seen the emergence of standards such as PCIe (Peripheral Component Interconnect Express), XAUI (10-Gbps attachment-unit interface), SATA (serial-advanced-technology attachment), USB (Universal Serial Bus) 3.0, and GbE (gigabit Ethernet), among others.

Both the serializer and the deserializer functions rely on PLLs to generate their clocks. The serializer requires a low-jitter, frequency-multiplying PLL for the transmitter. The PLL multiplies the parallel-rate clock frequency up to the serial rate. A multiplication by 10 to the parallel rate is common. The serializer PLL typically specifies less than 1% rms (root mean square) of the clock period for long-term jitter—for example, 1 psec rms at 10 Gbps.

The receiver requires a CDR (clock-and data-recovery) circuit, a type of PLL that locks to incoming data rather than to a clock. CDR circuits have for decades found use in optical communication. However, CDR circuits have only in the last decade become small enough and low enough in power to make integrated SERDES practical.

One of the first integrated CDR circuits was part of a 2.488-Gbps chip set whose developers fabricated it in gallium-arsenide and silicon-bipolar technology (**Reference 5**). It used an external loop filter and an external transmission line for the resonator in the VCO. In the 20 years since this integrated CDR debuted, the same advancements that have helped other types of PLLs have helped CDRs to shrink in power and area. Standard CMOS-logic processes integrate CDRs that require no external components and consume much less than 1 mm^2 of chip area.

The miniaturization of PLLs opens many other types of applications to these devices. Common examples include deskewing PLLs, which align the clock at the end of a clock tree with an input clock, and multiphase PLLs, which generate four to 32 output clocks with equally spaced phases and find use in RF receivers and multichannel CDR circuits.

PLLs have come a long way since the emergence in the 1970s of monolithic PLLs. Much of this advancement has come from the improvements in process technology. Further improvements in performance have come from innovative circuit-design techniques. With these developments, PLLs have become versatile and essential building blocks. Modern SOCs, such as multimedia processors, contain eight to 20 PLLs performing diverse functions. As technology advances, PLLs will find use in even more applications. EDN

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AUTHORS' BIOGRAPHIES

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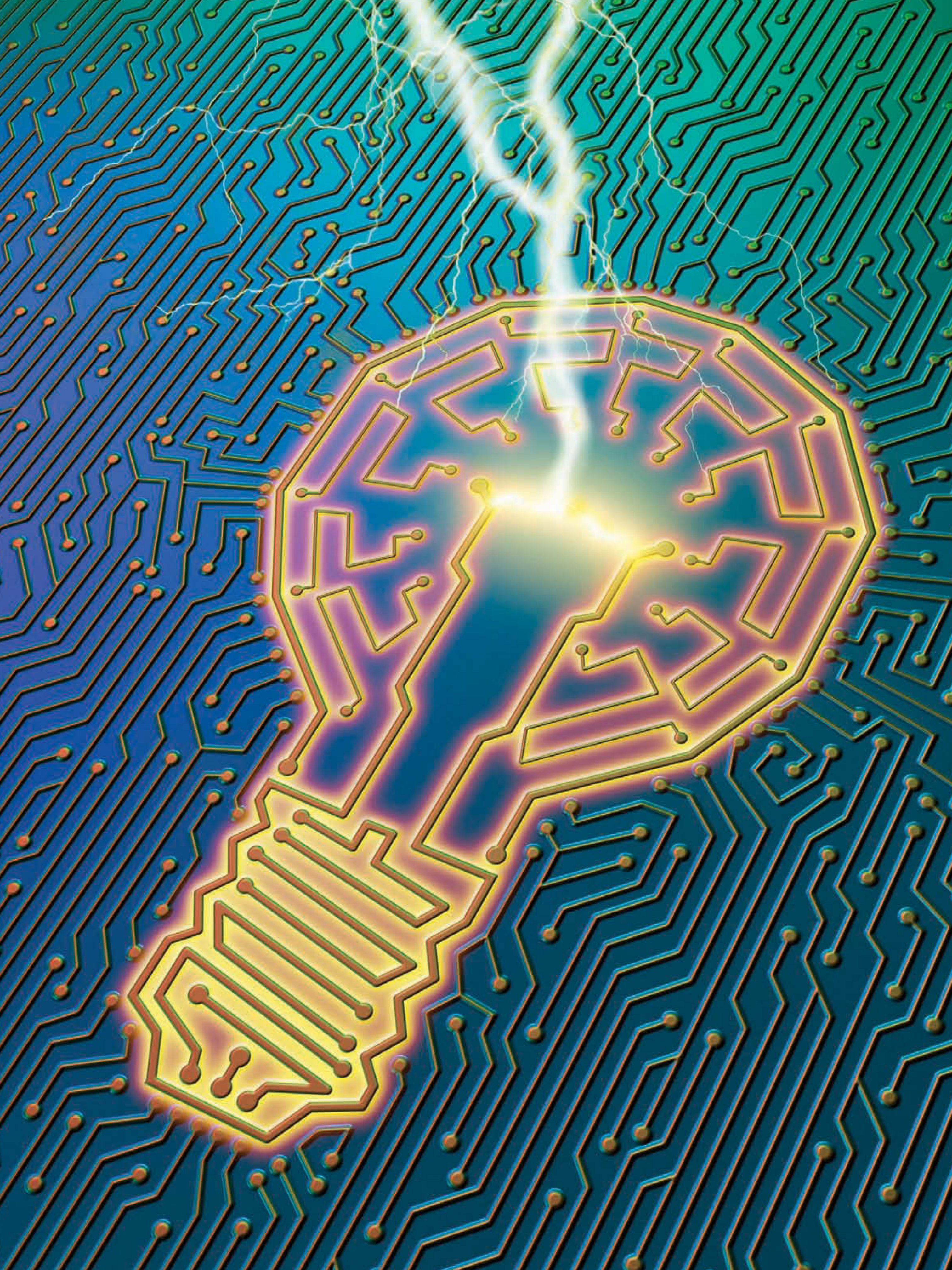
POWER-INTEGRITY SIMULATION KEEPS YOUR PLANES PERFECT

BY PAUL RAKO • TECHNICAL EDITOR

SIMULATE THE POWER-DISTRIBUTION NETWORK IN YOUR PCB TO ELIMINATE THERMAL AND VOLTAGE PROBLEMS.

Delivering power to the chips on your PCB (printed-circuit board) is no longer a simple proposition. You used to be able to connect the ICs to power and ground using thin traces that took little space. As chips got faster, you fed them power with low-impedance sources, such as a power plane on your PCB. For a time, just using a power and ground plane on a four-layer board would solve most power-integrity problems. In addition to the power planes, you could decouple every IC to solve any niggling power problems with your design.

IMAGE: MASTERFILE



These days, though, PCB areas—along with their cost and your schedule—are tight, and these issues bring power consequences along with them. "Consumer and portable devices are using fewer PCB layers for cost, but the ICs inside them need many voltage levels," says Dave Kohlmeier, senior product-line director of simulation and analog at Mentor Graphics. These problems don't apply just to portable products; industrial products have space constraints, too (**Figure 1**). A modern cell-phone base station has circuitry in a small box on the antenna that used to reside in a 19-in. rack in the building.

Cost is critical in high-volume consumer and automotive products. You can't afford to sprinkle your PCBs with capacitors that they might not need. To top it off, your design cycles have shrunk to weeks and months instead of years. You can't take the time to do respins of your PCB to fix and optimize the power and ground planes.

Designing power systems for modern electronics is a daunting challenge. DDR memory operates at 1600 Mbps and will soon run at 2200 Mbps in quad mode. Worse yet, it is a single-ended output, meaning that your power system must deal with sudden changes in power-supply current. Digital gates in the part can all switch at once, a feature that power-integrity engineers characterize as simultaneous-switching noise. Serial communication has difficult power demands. The 802.3ba Ethernet standard calls for 40- and 100-Gbps data rates (**Reference 1**).

Modern digital chips operate on less than 1V, meaning that even millivolts of noise can cause data-dependent problems. Multiple chips can add statistically and cause power dropout or overvoltage. Your system might work fine for weeks or even months until the digital circuitry all switches at once, causing a system reboot. These power-integrity problems are difficult to troubleshoot. Power-integrity problems on one chip in a system may cause another chip in the system to reboot. "Even a nanosecond of power loss will make your system unreliable," notes Paul Grohe, an analog applications engineer at National Semiconductor. Minimizing power-supply noise is critical to your design's reliability, meaning that digital-system engineers must learn analog and even RF-design concepts, according to Steve Patel, signal-integrity-product manager at Ansys.

AT A GLANCE

- Simulate dc power integrity to ensure that your power planes can carry the required current.
- Simulate ac power integrity to ensure that your design has adequate decoupling.
- Software lets you simulate the effect of stitched power and ground planes.
- Inadequate copper can cause severe thermal problems on your PCB (printed-circuit board).
- Power-plane noise can ruin your signals.

Power-system engineers know that power systems must have low impedance (**Figure 2**), and analog engineers understand that the less noise on the power pin of an analog IC, the better. Unlike digital chips, analog chips have no noise margin. The PSRR (power-supply-rejection-ratio) specification tells you how much of the power-supply noise will seep into the part's output pin. Digital-system engineers must now deal with the same power-noise issues (see **sidebar** "Let me talk to someone else").

The power-delivery network that supplies your chips requires low equivalent inductance—0.01 nH for core voltages and 1 nH for I/O power, according to Brad Brim, product marketing manager at Sigrity. He notes that the power planes couple noise back into your signals. In some cases, a signal routed between two ground planes has

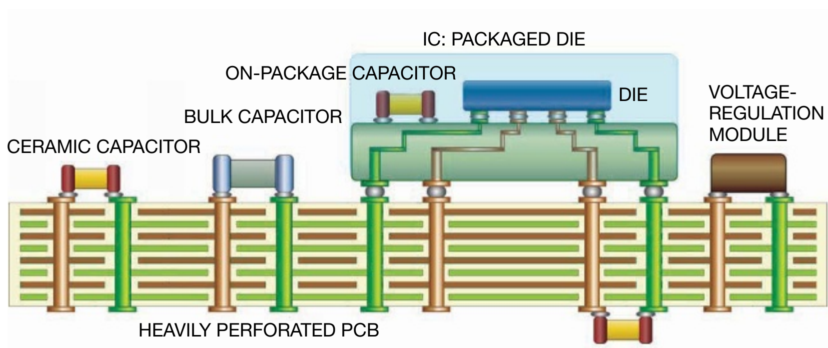


Figure 1 Packing more components onto smaller PCBs results in heavily perforated power and ground planes with the attendant power-integrity problems (courtesy Agilent).

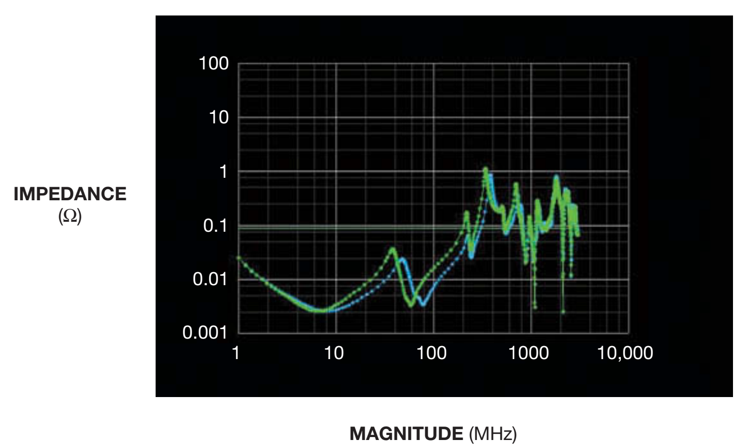
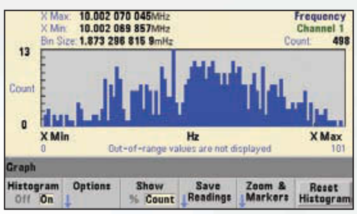
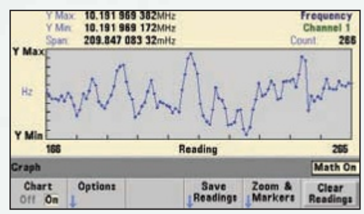


Figure 2 Minimizing the ac impedance of your power planes over all frequencies is critical in high-speed circuitry. This simulation shows planes with impedances as high as 1Ω (courtesy Mentor Graphics).

"I never expected a frequency counter to do so much, so fast."

Speed, resolution and accuracy are just the beginning.





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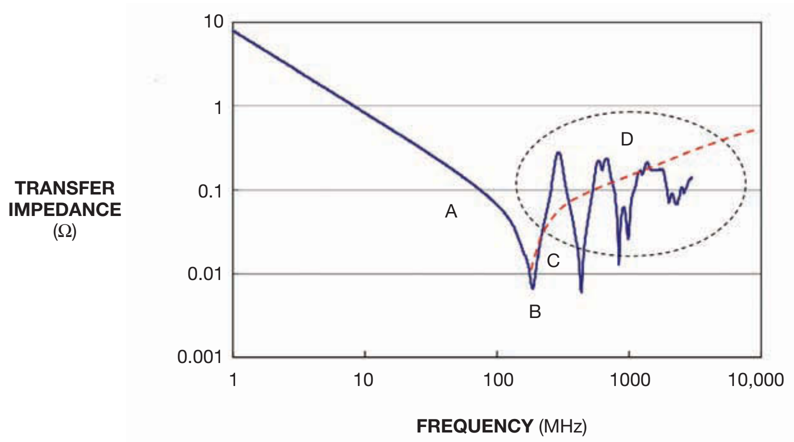

Figure 3 An idealized plot of power-delivery-network transfer impedance has a capacitive region (Point A) and an area in which capacitive and inductive reactance are equal (Point B). As frequencies increase, inductive reactance effects predominate (Point C). A perfect idealized plane would follow a smooth line (red). Instead, the dielectric constant and the plane geometry create plane-resonance modes (Point D) that ruin power integrity (courtesy Sanmina-SCI).

15 mV of noise. When the layout person routed the same signal between the power and the ground planes, it had 45 mV of noise.

Power-integrity tools let you make a deterministic optimization of your design. You cannot use accepted rules of thumb for decoupling to optimize the layout. Software helps you to determine the number, type, and cost of capacitors, says Ansys' Patel. These tools also show you the effect of changing the distance between planes. For example, NEC's PI (power-integrity) Stream helps you meet your target impedance by adding or moving capacitors, changing capacitance values and plane shapes, and altering the distance between power and ground planes, says Yoshi Fukawa, president and founder of TechDream.

"You can use a CAD file for what-if experimentation," says Mentor's Kohlmeier. "It is much faster than hardware spins. That is the value of a virtual prototype." For these reasons, it is important to use simulation software so that you can make important decisions early in the design phase. Capacitor location, capacitor count, and other variables might not affect other departments, but changing the thickness of the board because you moved planes closer to gain interplane capacitance affects the whole design team (**Figure 3**). Sanmina-SCI has patented modern manufacturing methods that let you design planes with 4-mil-thick dielectrics, increasing interplane distributed capacitance.

PROBLEM SOLVER

Power-integrity simulation is more difficult than many engineers expect because they must account for every capacitor, stitching via, and structure in the power-delivery plane, says Kohlmeier. He points out that stitching vias, which connect two planes, lower the impedance of your power-delivery network and, as such, are just as important as capacitors.

Unlike power integrity, signal integrity usually involves a few traces, and you can measure signal integrity in the time domain with an oscilloscope. Power-integrity simulation yields frequency-domain impedance using the Z11 profile of the impedance from Port 1 to Port 1. To understand the impedance problems of a power plane, you need a VNA (vector network analyzer), which is difficult to use. Simulations are complements, rather than replacements, of measurements, and they provide important information about the performance of the PCB before fabrication. "No matter how fast your simulation software, nothing is faster than a measurement," says Sigrity's Brim, who notes, however, that you need a fabricated PCB on which to take that quick measurement.

LET ME TALK TO SOMEONE ELSE

Power-integrity-design engineers have a problem talking to digital-system engineers who have no knowledge of power-design concepts. For example, Bob Thomas, a senior power engineer at Cisco Systems, relates that he often becomes exasperated talking to the digital-design engineers who work for the FPGA companies from which Cisco buys chips. These digital-design engineers just don't speak the language of analog- and power-system designers. In one case, a digital-system engineer told Thomas that a chip needed a power-noise spec of –20 dB. "A decibel is a relative measurement: 20 dB down from what?" he asked. The other engineer just insisted that the power noise had to be –20 dB.

Thomas knew it couldn't be dBm (decibels referenced to milliwatts) or some other power measurement. "I need to talk to someone else," he said. The digital engineer protested but finally put another engineer on the phone. That engineer also could not give Thomas a reasonable spec. "I need to talk to someone else," Thomas said. It took about four people, but the FPGA vendor finally got someone on the phone who spoke the language of analog-power design. Once Thomas got a valid power-noise spec from that engineer, he proceeded with his design.

Remember this anecdote when you deal with digital-chip vendors. They have the best intentions and want to help you, but be sure that you are talking to someone who understands the analog care and feeding of digital chips. It is guaranteed that the digital-chip company has a person like that on the payroll; you just have to seek him out.

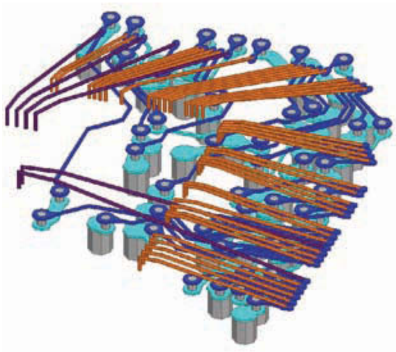

Figure 4 The bond wires inside an IC are in parallel and have low impedance (orange). The PCB traces you connect to those pins (blue) are more troublesome. For clarity, the IC die is not shown (courtesy Ansys).

You must trust that the IC designers have done their job and that the chips you use have no power-integrity problems. "ICs and their bond wires are not that critical in power integrity," says Ansys' Patel, because IC power pins and bond wires are all in parallel (**Figure 4**). Instead, the layout engineer, who may lack the technical knowledge to avoid power- and signal-integrity problems, determines the power plane's shape, often causing the problems, according to Steve Kaufer, engineering director for HyperLynx at Mentor Graphics

Power-integrity software helps you with dc and ac problems, as well as with the fact that the cavities between the power and ground planes are RF waveguides. To deal with the dc problem, you must ensure that the PCB planes can carry the current they must deliver. To deal with the ac problem, you must ensure that the power system can deliver the fast transient currents that modern chips require. Finally, note that the behavior in the waveguide may be nonintuitive. This RF aspect is important in preventing EMI (electromagnetic-interference) problems that will cause your board to fail FCC (Federal Communications Commission) certification. It is important to use simulation if your design has large planes, which can resonate. Adequate software simulation can help your EMI engineer solve problems if your planes spew RF from the interplane cavity. The fix might involve placing capacitors around the edges of the board. Sun Microsystems has patent 6727780, which uses resistors in series with capacitors so RF energy is absorbed at the edge of the board instead of reflected back into the structure.

The digital chips require high currents, which may cause dc-power-delivery problems (**Reference 2**). FPGAs and other digital chips need many power-supply voltages, so you must divide your power planes to deliver multiple power rails. Digital chips also have hundreds of pins whose fan-out traces require hundreds of vias that wipe out large areas of copper in power and ground planes. You must ensure that the current density in the copper you select for the planes stays below a reasonable value (**Figure 5**).

High dc current also causes thermal problems. The temperature coefficient of copper is 0.4%/°C, meaning that it adds 10% more resistivity for every 25°C increase in heat. That increase in resistance occurs under heavy loads, when reliability is critical. The increase in resistance also increases temperature, reducing the lifetime of the components on the board.

Once you have enough copper to supply the dc load, look at the ac design of the power plane (**Figure 6**). Power-integrity simulation lets you examine where the return currents flow in your planes. During operation, a digital chip draws radically different current levels, which change in nanoseconds. Your

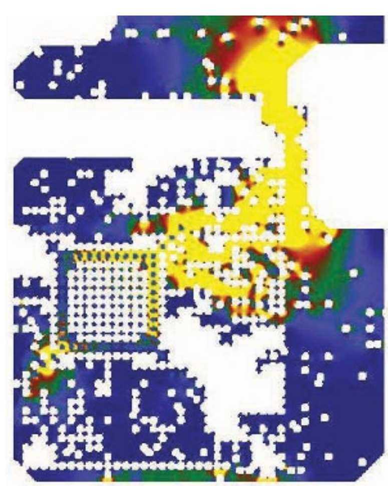

Figure 5 With power planes so convoluted on modern PCBs, it is important to check that there is enough copper to carry your required current. The yellow areas in this simulation have insufficient copper (courtesy Mentor Graphics).

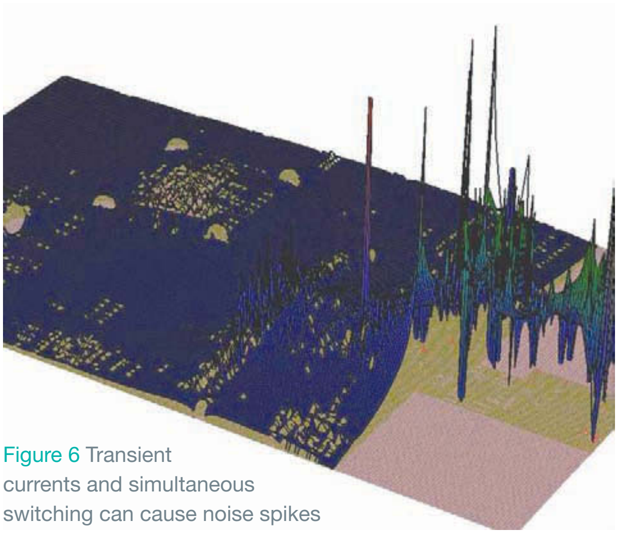

Figure 6 Transient currents and simultaneous switching can cause noise spikes on power and ground planes (courtesy Mentor Graphics).

power system must have low enough ac impedance that the large changes in current, expressed as di/dt (derivative of current over the derivative of time), do not create large power-supply-voltage changes at the chips' pins. Because di/dt also radiates electromagnetic energy, these excursions can cause EMI problems. As a result, signal integrity, power integrity, and EMI compliance all interrelate. Without simulation, your design may experience via-to-via crosstalk and other issues that might seem inexplicable.

SOFTWARE CHOICES

The physical geometry of a power network is critical to its performance, so most software vendors use field-solver technology in their power-integrity tools (**Reference 3**). These tools should give you a fast answer and accurate results. RF-IC and system designers routinely use full-wave field solvers to solve Maxwell's equations in 3-D. However, 3-D field solvers take a long time to achieve a result, especially if you apply them to a relatively large physical item, such as a PCB. Accordingly, power-integrity vendors design hybrid solver technology into their power-integrity tools. While solving for traces, these tools might use a 2-D solver with a fast technique employing transmission-line theory. For simulating planes, the tools can use 2-D or 2.5-D finite-element techniques. In some cases, the software can model vias using a lumped-element capacitor and inductor model. The tools apply a full-wave 3-D solver to the vias for accurate results.

You would also use a full-wave solver to simulate the effect of 3-D structures, such as connector pins and other mechanical devices in the power path. Software vendors also put thermal analysis in their tools. You can use this feature alone or export the thermal information to a specialized thermal-analysis tool, such as Mentor Graphics' FloTherm, a CFD (computational-fluid-dynamics) 3-D simulation environment. Mentor's HyperLynx simulation tool can do its own thermal analyses and export the results to FloTherm so that you can model the thermal performance of an entire system or an enclosure.

Agilent has re-engineered its ADS (advanced-design-system) Momentum product to provide simulations results when you have heavily perforated power and ground planes. It also accommodates designs that need a few signal traces in the

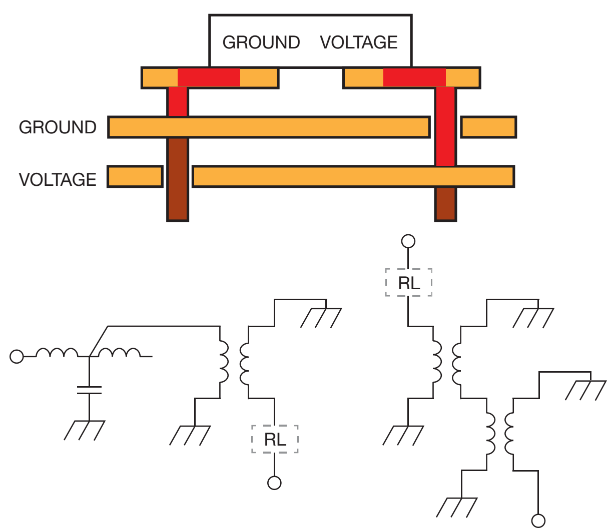

Figure 7 You can model the impedance of the part connections to voltage and ground planes using a lumped-element approximation. The RL element is a series resistance and inductance (courtesy TechDream and NEC).

FOR MORE INFORMATION

Agilent Technologies
www.agilent.com

Altium
www.altium.com

Ansys
www.ansys.com

Cadence
www.cadence.com

Cisco Systems
www.cisco.com

Computer Simulation Technology
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Giga Hertz Technology
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Mentor Graphics
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NEC Informatec Systems
www.nec-nis.co.jp/emistream/pistream/

Sanmina-SCI
www.sanmina-sci.com

Sigrity
www.sigrity.com

TechDream
www.tech-dream.com

Zuken
www.zuken.com

planes. MOM (method of moments), the fastest simulation method for multilayer structures, solves full 3-D fields, including all of the terms in Maxwell's equations. This full-wave approach accounts for the high-frequency effects of Faraday's Law and the displacement current term that Maxwell added to Ampère's Equation (**Reference 4**). Using MOM to simulate large planes is time-consuming, so Agilent invented algorithms that reduce the time necessary for achieving accurate results. The tool works down to dc using a tree/co-tree method, according to Colin Warwick, product owner for high-speed digital at Agilent.

You can also adapt lumped-element analysis to planar elements. NEC's PIStream software models planes as matrices of lumped elements, making it suitable for analysis using Spice engines and other lumped-element techniques. For a plane, the software generates an RLGC (resistance/inductance/conductance/capacitance) equivalent using the PEEC (partial-element-equivalent-circuit) technique. The software similarly generates lumped-element models for the vias and cavities that form between the ground and the voltage planes (**Figure 7**). The software also models a decoupling capacitor using a series RLC (resistance/inductance/capacitance) model that combines the parasitic resistance and capacitance of the capacitor with the parasitic resistance and inductance of the fan-out traces and vias. You can set up a simulation run to quickly perform single-pair analyses. When you change settings, the software will perform a multilayer analysis that takes into account all relevant planes.

In addition to simulating the physical configuration of finished boards, a software tool such as HyperLynx lets you perform early-stage floorplanning of your planes and decoupling structure. You can then quickly run an analysis to give you some idea of the transfer impedance and other variables. Giga Hertz Technology has developed a faster Spice engine and integrated it into NEC's PDN (power-delivery-network) Expert. With these floorplanning tools, you can manually sketch the PCB and plane and optimize the capacitors earlier in the design. Thus, you get an idea of the plane's shape, size, stackup, and capacitor count.

Some power-integrity-software vendors from the PC world, such as Mentor Graphics and Cadence, integrate their tools into the design flow. Although it is reassuring to have one vendor supplying all the tools, the power-integrity simulation uses a physical representation of the PCB and makes a geometric model. Ansys and Sigrity both accept inputs from Cadence's Allegro; Mentor Graphics' PADS; and tools from Zuken and Altium. Agilent derives its power-integrity tools from its significant expertise in RF design. In addition to working with the ADS design tool, the company's EMPro software can import PCB data from Cadence's Allegro. Customers often use NEC's PIStream with Zuken's PCB tools, but the software can accept inputs from Cadence's Allegro and other PCB software.

Although some engineers prefer that their board flow has integrated tools, getting tools from a simulation expert, such as Ansys, has some advantages. For example, the company's SI (signal-integrity) Wave tool is similar to Mentor Graphics' HyperLynx, and a PIAdvisor tool helps you delve into power-integrity issues. The tools have 3-D solvers for simulating vias. You can also use the Ansys HFSS (high-frequency-simulator-system) tool for full 3-D simulations of physical problems, such as connectors and other 3-D geometry. Some customers import the output of the Ansys power- and signal-integrity tools to the same HFSS tool they use to model the enclosure. In that way, they can evaluate their product's EMI. CST's (Computer Simulation Technology's) EM Studio software imports Gerber PCB files and can calculate 3-D IR (current/resistance) drop.

The software you select must have the capabilities you need. Many companies expect that you will solve the signal- and power-integrity problems separately, assuming that, once you sufficiently reduce the power impedance, you will then look at signal integrity. The problem with this approach is that power and signal noise interacts. To offset that problem, Sigrity allows you to simulate the effect of power noise on signal integrity (**Figure 8**). CST's Microwave Studio also lets you analyze noise propagating from power planes in close proximity.

STICKER SHOCK

The price of power-integrity software often shocks inexperienced engineers. A simple dc simulator can cost $15,000, and a full-blown system with power-integrity, signal-integrity, and thermal solvers can cost as much as $75,000. This figure may seem high for software until you consider the costs of power-integrity failure. A complex board spin can cost $5000 or $10,000 in fabrication and engineering and $1 million in time-to-market expenses. Another consideration is the BOM (bill-of-materials) cost of your system. If your power-integrity software can save you 50 cents in capacitors, you could recover the cost of the power-integrity software in a few months for a high-volume product.

Ansys' Patel observes that three engineers once did power-integrity, signal-integrity, and EMI analyses in isolation. These days, although one engineer may do EMI analysis, that person first works with a person who performs both power- and signal-integrity analysis, and they often all share the same software. Sigrity's Brim notes that IBIS (input/output buffer specification) 5.0 has power-ground and signal data that allows your simulation software to relate the noise on the power pin of a 5.0 model to the noise that leaks through to the output, similar to the PSRR spec in an analog part. All of these features combine into one unified effort to give your company a solid, well-designed product (**Figure 9**).

If you understand and know how to use these expensive tools, your worth as an engineer increases. Learning the tools is not hard for engineers who embrace CAD (computer-aided-design) software. Mentor Graphics offers free workshops for HyperLynx at many of the company's sales locations. If you are experienced with other types of simulators, you will have little problem learning power-integrity tools. You need to learn and understand the concept and lingo of the frequency domain, just as an RF designer does. By adding that knowledge to your time-domain expertise, you can take on the toughest design challenges and come out a winner. EDN

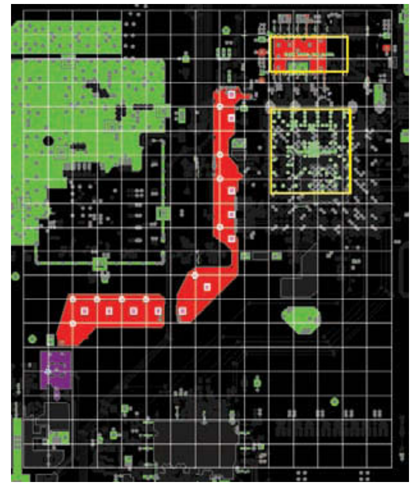

Figure 9 A narrow power plane (red) is difficult to properly decouple. Software can help you locate the 11 decoupling capacitors in strategic places (white). This approach works better and uses fewer capacitors (courtesy Sigrity).

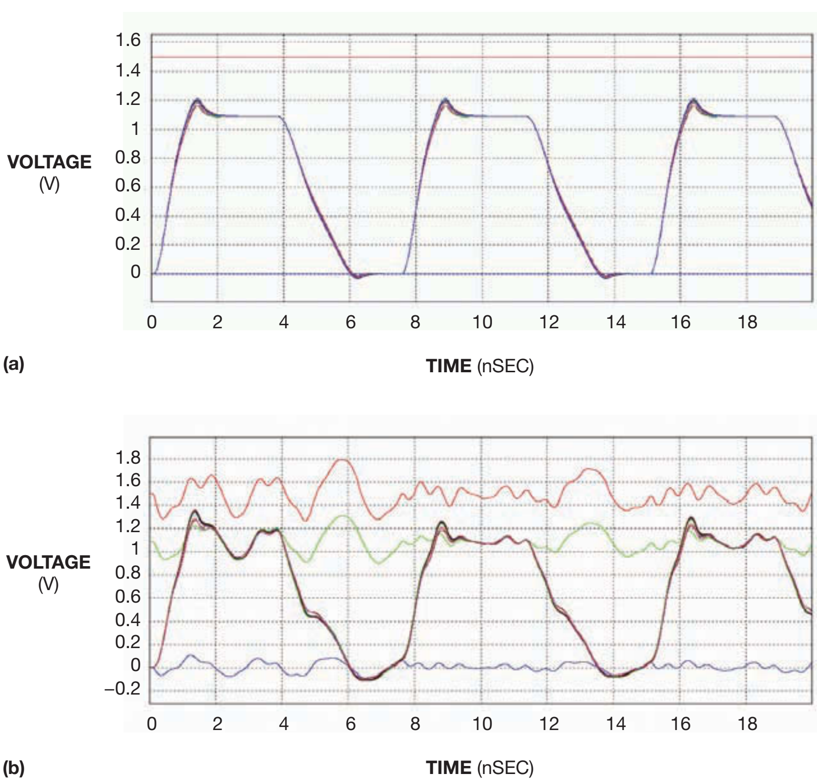

Figure 8 If your simulation software assumes ideal power (red), the signal excursions to ground (blue) will look much better than reality (a). Once you add in the noise on the power and ground planes (b), you can see a significant effect on the signals to both low levels (blue) and high levels (green, courtesy Sigrity).

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3 Rako, Paul, "Beyond Spice: Field-solver software steps in for modeling high-frequency, space-constrained circuits," *EDN*, Jan 18, 2007, pg 41, http://bit.ly/bzMUen.
4 "Shortcomings of the original formulation of Ampère's circuital law," http://bit.ly/lg6ji2.

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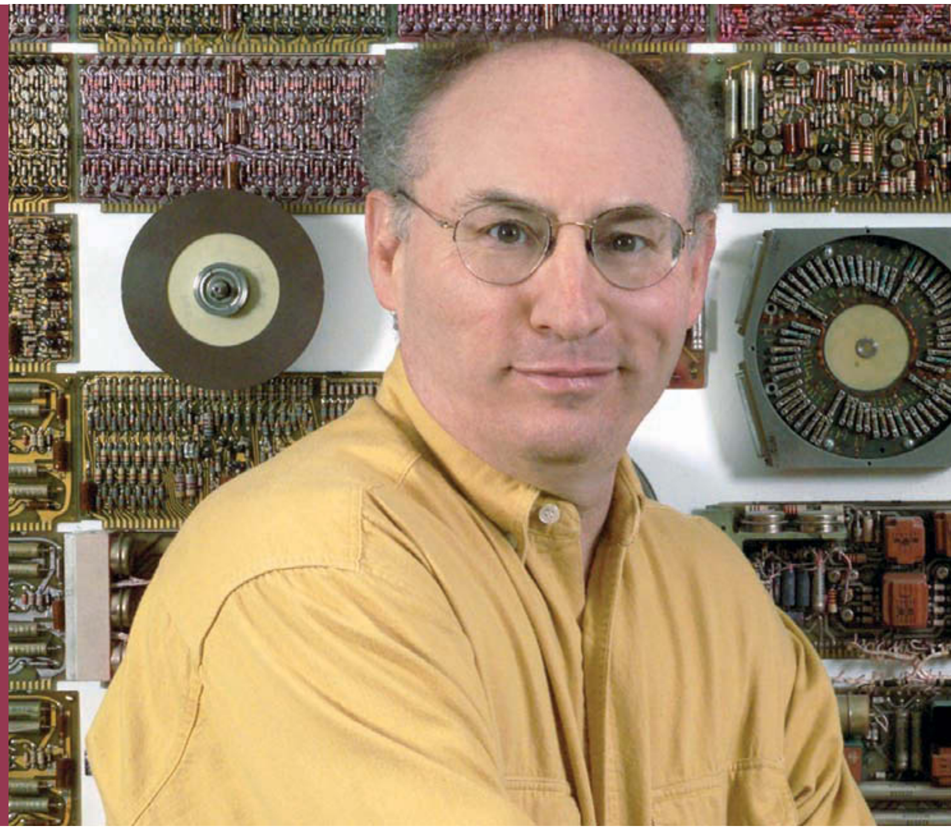


Art and design: Jim stands in front of a creative spread he did of the innards of a Minuteman missile, which hangs in his living room (courtesy Linear Technology)

GONE BUT NOT FORGOTTEN

ANALOG GURU JIM WILLIAMS

EDN'S PAUL RAKO, INDUSTRY EEs, AND OTHER CO-WORKERS AND FRIENDS REFLECT ON THE LIFE AND WORK OF JIM WILLIAMS, AN ENGINEER'S ENGINEER AND ANALOG EXPERT, WHO DIED UNEXPECTEDLY ON JUNE 12, 2011, AFTER A STROKE.

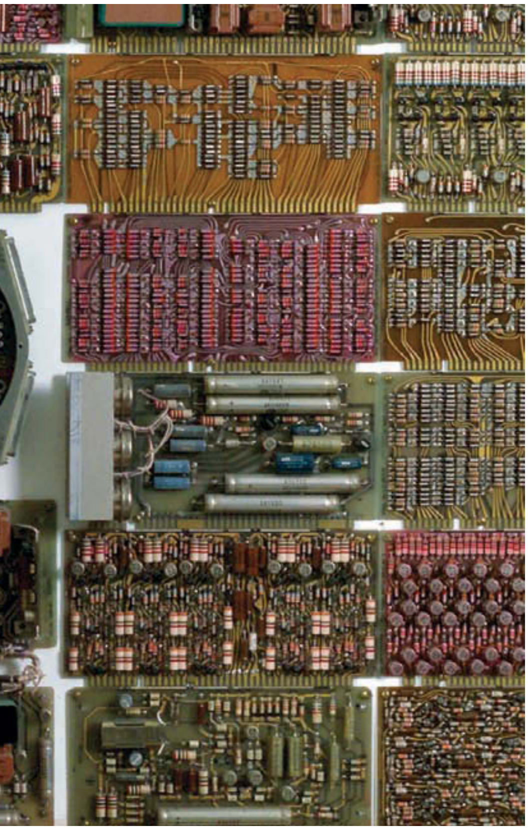
BY PAUL RAKO • TECHNICAL EDITOR

World-famous analog guru Jim Williams, who helped found and expand Linear Technology Corp, passed away peacefully at Stanford Hospital, Stanford, CA, in the company of family and friends at 10:15 p.m. on June 12, two days after suffering a massive stroke. Along with his wife, Siu, and son, Michael, he leaves behind an analog community—and electronics industry at large—enriched by his many contributions, both personal and technical, that will continue to ripple for decades to come.

Jim had just returned to work from a well-deserved vacation and was excited about his next two articles for *EDN*. One, concerning sine-wave oscillators, is currently slated for the Aug 11, 2011, issue; the other will be his last article for *EDN*: a brilliant description of developing a 100A electronic load, currently scheduled for the Sept 22, 2011, issue. No one imagined at the time the article was submitted that it would be his last for a publication whose relationship with Jim goes back more than 35 years.

Jim was pleased with that article. He often told me that it was one of the few technical projects in which "everything just worked perfectly." He said it was rare to have all the parts of a complex design go so well. When he confided this feeling, I couldn't help but think how his awesome talent had to play a part in the ease of the design.

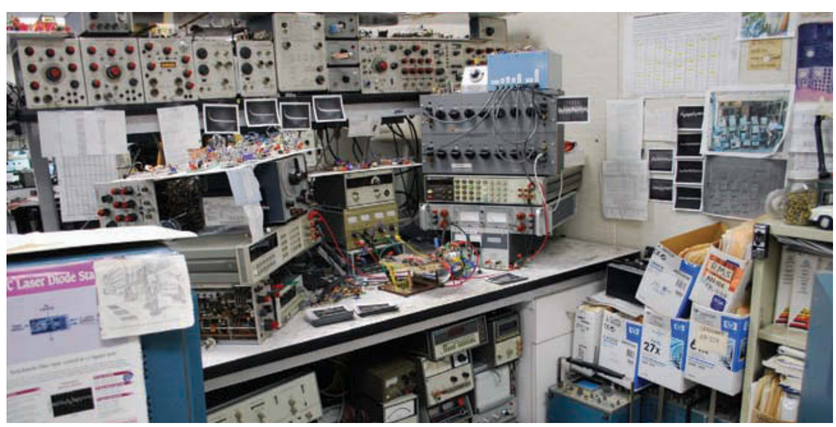
Jim's background was as interesting as the circuits he designed. You might say that he "lacked credentials." He took one semester of psychology at Wayne State University in Detroit. When Jim was growing up, however, a neighbor shared with him his garage full of big, beautiful Tektronix oscilloscopes. As a result, Jim developed a passion for electronics, and especially for test equipment. His passion led him to the Massachusetts Institute of Technology—not as a student but as a lab technician who built hardware for the scientists and kept a slew of sophis-

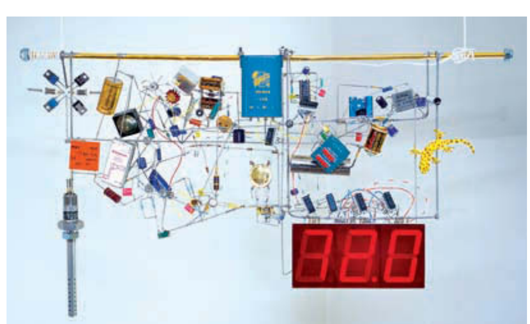


ticated test equipment working. The department head once told Jim that a certain piece of equipment was beyond repair. That's all Jim needed to hear. Always up for a challenge, Jim fixed it in three weeks.

Test equipment must be more advanced than the circuits it tests, so learning the design of test equipment turned Jim into one of the best analog engineers in the world. He never confused description with understanding. When he gave seminars on how to design piezoelectric-transformer lamp drivers, he pointed out that professors who fill the blackboard with math don't know how a circuit works. He believed that, although math can describe how a circuit works, *understanding* how it works is a more fundamentally intuitive and poetic endeavor.

In 1975, while still working for MIT, Jim wrote his first article for *EDN*, "Heavy-duty power supply regulates either voltage, current, or power" (available online on the Jim Williams archive page at www.edn.com/jimwilliams). The article, like those that followed, stressed the need for a deep understanding of underlying concepts. Jim neither talked down to his readers nor tried to show off. A brilliant teacher, he simplified things





This page (top to bottom): Jim and his wife, Siu; young Jim at Linear Technology; Jim at work at his lab bench; one of Jim's four lab benches at work; one of Jim's many electronic sculptures (courtesy Fran Hoffart) until you understood them, and he made things look simple. Anyone can learn jargon and a few tricks and secrets to try to look smarter than they are. Jim was the exact opposite. He painstakingly described the basic principles of operation of the topic he was discussing—be it how application engineers should serve the customer (June 25, 2009), measuring settling time (March 4, 2010), or designing an acoustic thermometer (April 21, 2011). He then showed you how to achieve your goals for your designs.

Jim loved to get his hands dirty, hacking on copper-clad boards and brandishing a soldering iron rather than instructing a technician about how to perform these tasks—a great example for generations of analog engineers. He taught us all that doing the work yourself gives you a far deeper understanding of the design than if you just toss a schematic to a hapless technician.

"Jim lived electronics," says Bob Dobkin, founder of Linear Technology and the victim of many of Jim's pranks. "Electronics—along with humor—was his art." Jim's belief in building your own prototypes and testing them taught tens of thousands of engineers the right way to get a working design from scribbles on a paper napkin to production.

For one so brilliant, Jim was modest, quiet, and articulate. His joining Linear

EETimes editor Bill Schweber also published a touching tribute to Jim: www.edn.com/110714df2a.

View additional photographs of Jim in the *EETimes* photo gallery at www.edn.com/110714df2b.

Technology in the earliest days also made him wealthy, but it was hard to tell from his manner. He was never condescending, despite his wealth and talent. Jim loved to talk to fellow engineers, and he meant *talk*. He had no use for e-mail, a cell phone, or voice mail. It was OK for engineers, readers, or editors to call him while he was at work, though. He especially welcomed hearing from fellow engineers, saying that he learned as much from them as they could learn from him.

Jim had a window office with a door, but calls to his office phone almost always landed at the lab bench where he spent most of his time. He respected the best in people. He didn't care what country you came from, what car you drove, or what breakfast cereal you liked. All Jim needed to know was that you loved analog. He was approachable and friendly, no matter what the situation.

In the late 1970s, Jim worked in the Boston area—for Teledyne Philbrick, Arthur D Little, Consultek, and Analog Devices. By the late 1970s, however, the action in electronics was in Silicon Valley, so Jim went to work at National Semiconductor. "We tried to get him to stay in Boston, but the call of the West and all that action was too much to beat," says Dave Kress, a former coworker at Analog Devices.

While Jim was at National Semiconductor, several engineers left to form Linear Technology, but Jim didn't go with them. "They didn't have any chips yet," he said. "What did they need an application engineer for?" That situation soon changed, however, and Jim joined Linear as the company's first applications person.

"Jim and I were good friends, even at a distance and working for competitors," says Kress. "But we never personally felt competitive. He was extremely creative and productive."

Dobkin encouraged Jim to write for the trade press, to demonstrate the capabilities of Linear Tech's parts. Beyond achieving that goal, though, Jim's articles also demonstrated his brilliant command of analog design. He wrote 60 articles for *EDN* during the 1980s alone. His natural emphasis on analog gave *EDN* an analog tilt that continues to this day. Loyal readers knew they could learn the best principles of analog design by just reading his articles. Despite suffering from Parkinson's disease, Jim never let it slow him down or affect his prodigious output of work.

Jim's effect was profound. Alan Martin, himself a brilliant engineer, read Williams' articles, which instilled in him a love of analog. As a result, Alan moved from Colorado to Silicon Valley and took a job at Linear Tech—just so that he could work with Jim on a daily basis.

Jim had that effect on every engineer around him. He made you want to do the best work you could. He made you want to solve the intractable problems. He made you want to not just get it working but to get it working in an elegant way. Jim helped set the standard for analog engineers the world over. That world will miss his technical brilliance and his warm personality. I know I will. **EDN**

Jim leaves his wife, Siu, and son, Michael. You can make donations in his memory to The Parkinson's Institute, 675 Almanor Ave, Sunnyvale, CA 94085.

Jim's first article for *EDN*, "Heavy-duty power supply regulates either voltage, current, or power," was published on May 5, 1975. Read the article online at www.edn.com/jimwilliams. During Jim's decades-long association with *EDN*, he wrote numerous additional articles, many of which also can be found on the Jim Williams archive page at www.edn.com/jimwilliams. Below is a sampling of some favorites:

- "Something from nothing," Sept 15, 2005
- "JFET-based dc/dc converter operates from 300-mV supply," May 25, 2006
- "1-Hz to 100-MHz VFC features 160-dB dynamic range," Sept 1, 2005
- "20-bit DAC demonstrates the art of digitizing 1 ppm, part 1: exploring design options," April 12, 2001
- "The taming of the slew," Sept 25, 2003
- "A clock for all reasons, part 1: monolithic oscillator invigorates instrumentation applications," June 26, 2003
- "Thank you, Bill Hewlett," Feb 1, 2001
- "Precisely measure settling time to 1 ppm," March 4, 2010
- "An introduction to acoustic thermometry," April 21, 2011
- "Layout and probing techniques ensure low-noise performance," Feb 2, 1998

FAMILY, FRIENDS, CO-WORKERS, AND *EDN* READERS HONOR JIM

Numerous people who had the pleasure of knowing Jim both personally and professionaly responded to the news of his death with an outpouring of stories and favorite memories of Jim. These comments are a true testament to Jim's life and work. Below is just a sample. Read more online at www.edn.com/110714df2c:

"As Jim Williams' son, nothing has been more touching and comforting than being able to read about how much he will be missed by all those that knew of him or were fortunate enough to work with him. … My father was a brilliant and ingenious man, but what most people do not know is that he was also an excellent father. … He expected me to stick to my word, treat people with respect, and, most important, to be loyal and honest to myself and to those around me. … His loyalty, generosity, and moral discipline were only outranked by his ability to make me feel like the proudest son in the world. … I will never forget our times together, whether we were driving around in his Jaguar XKE with the top down or discussing our love for vintage electronic equipment over hamburgers. You could find us on weekends at the De Anza electronics flea market or watching the Niners take a pounding on TV. Whether he was giving me advice on my love life or teaching me how to find the fuel cap on a '56 Chevy, I always listened, eager to learn everything I could from him. I love you and miss you, Dad."—*Michael Williams*

"Original. Generous. Mentor. Friend.

For the past 23 years, Jim showed me how it should be done:

Saturday mornings at Foothill.

How to be a student of the past and use it as a guide to the future.

Why giant slide rules are cool.

The joy of a home lab and the beauty of growing up with a hobby and a job that are one and the same.

Funky electronic art.

How to pay attention to details and question every measurement.

How to write and speak with style and humor so that whether your audience is one or 1000, you are just being yourself.

How to mentor junior engineers with patience and grace, while helping them discover the same enthusiasm that you feel.

How to maintain scientific integrity and ignore politics.

How to give credit and praise when it is earned.

How to be ever mindful of the needs of other people.

How to live your life to the fullest by sharing what you love to do best with those around you.

Thank you, Jim."—*Bob Reay, vice president, mixed-signal products, Linear Technology Corp*

"Many years ago ... I needed an oscilloscope, and the obvious source for advice on anything lab-related was Jim Williams. I explained what I was looking for, and Jim said I was in luck: He had just bought a broken Tektronix 453 scope at the Foothill flea market. As I stood at Jim's bench, pondering exactly why I was 'in luck,' he reassured me that this scope would suit my needs and that he would have it fixed in no time. He offered to sell it to me for the $65 it cost him at the flea market; however, there were conditions attached.

A few days later, Jim brought the scope in to work and spent about five minutes explaining the features. He spent 10 minutes explaining how these features differed from those of comparable scopes, and then another 15 minutes explaining how to care for the scope. He showed me how to keep the tube in good condition and how to ensure that the filter for the cooling fan had adequate airflow. He explained how the past owners had taken good care of this instrument, and his first condition was that the new owner do the same.

Anybody who worked with Jim knew that he devoted as much care to the upkeep of his lab equipment as he did to the performance of his circuits. Few people will ever approach Jim's knowledge of electronic instrumentation. Even fewer will treat such instruments with the same level of care and respect. His final condition for parting with the scope was that it be used for something productive and profitable! Jim's devotion to his work and to the tools of his trade will be missed by all of us."—*Sam Nork, director, Boston Design Center, Linear Technology Corp*

"I have known Jim Williams for 30 years. I have known him as the consummate engineer, scientist, writer, humorist, and family man. In all areas that Jim ventured, he excelled. His combination of personal integrity, drive, and humble interaction with other people drew many friends.

Jim's intuitive understanding of electronics enabled him to design complicated circuits in his head, which he tested with real parts to prove the circuits. The ability to design circuits also requires analysis of the results of the testing. His strong analytical ability ensured test results were correct and circuits were well-understood.

Jim took his developments and turned them into words for publication. He helped engineers of all ages understand circuits intuitively like he did. There are few sources for advanced circuit understanding and design—especially the way it was taught by Jim. ... In all the time I've known Jim, I have never known him to refuse to help someone with a circuit.

While Jim's vocation, avocation, and hobby were electronics, he had a great sense of ... art. His electronic sculptures are unique, beautiful, and functional. He built these structures (with much cursing) and careful selection of aesthetically pleasing functional parts. He [also] had a great sense of humor, which was often foisted on his friends, myself included.

[Jim] was a dedicated father to his son, Michael, and husband to his wife, Siu. Both of these people were very much a part of his life. A successful poet is the rarest of all vocations. Jim Williams was unique: a poet who wrote in electronics."—*Bob Dobkin, co-founder; vice president, engineering; and chief technical officer, Linear Technology Corp*

BY ARCHANA YARLAGADDA • CYPRESS SEMICONDUCTOR

Simplifying multichemistry-battery chargers

PORTABLE ELECTRONIC DEVICES, WHETHER PERSONAL ELECTRONICS, REMOTE SCIENTIFIC INSTRUMENTATION, OR SIMPLE GARAGE FLASHLIGHTS, ALL HAVE ONE THING IN COMMON: BATTERIES. YOU CAN APPLY A FLEXIBLE BATTERY-CHARGING SYSTEM TO A RANGE OF VOLTAGES, BATTERY CHEMISTRIES, AND BATTERY-CHARGE PROFILES.

When charging multichemistry batteries with different cell capacities, the battery voltage can be higher or lower than the supply voltage at various stages of the charging. Thus, the supply voltage needs to be either boosted or attenuated to match the battery voltage. For example, a supply voltage of 3.3V must be attenuated, or bucked, when a single-cell NiMH (nickel-metal-hydride) battery with a typical voltage of 1.25V is being charged. When a single-cell, 4.1V lithium-ion battery is used, the input voltage needs to be boosted. To address such cases, you should use a SEPIC (single-ended primary inductor converter) as the primary charge path (**Reference 1**). This topology of switch-mode dc/dc conversion can both buck and boost a range of voltages to provide supply-voltage flexibility.

Lithium-ion and NiMH chemistries require different charge profiles, but you can easily use the same flexible charging topology for both. You implement the flexibility and simplicity in switching from one type of battery chemistry to another by using firmware on a microcontroller. By designing a modular charging subsystem and encapsulating functions into various modules, you can implement the same application using different microcontrollers in a family, depending on system requirements. The use of modules simplifies designs to allow developers to add battery charging to another main application, such as motor control and medical measurements (**Reference 2**).

To control the charging current, a battery charger must determine the battery's voltage, current, and temperature. The hardware to determine the state of the battery is common to the batteries, and the battery voltage can be higher or lower than the input range of the microcontroller. Thus, engineers usually measure the voltage using a resistor-divider circuit to attenuate the voltage. They can measure the current on the high side—that is, the current going into the battery; on the low side—that is, the current leaving the battery; or, in the case of SEPICs, by using a resistor in the secondary side of the inductor. The batteries usually have embedded thermistors that can be used to monitor and ensure the accuracy of the battery's temperature. Some commercial-battery manufacturers omit these thermistors to reduce cost. In such cases, users can place an external thermistor in contact with the battery.

Using these measurement parameters, the microcontroller determines and controls the charge current into the battery.

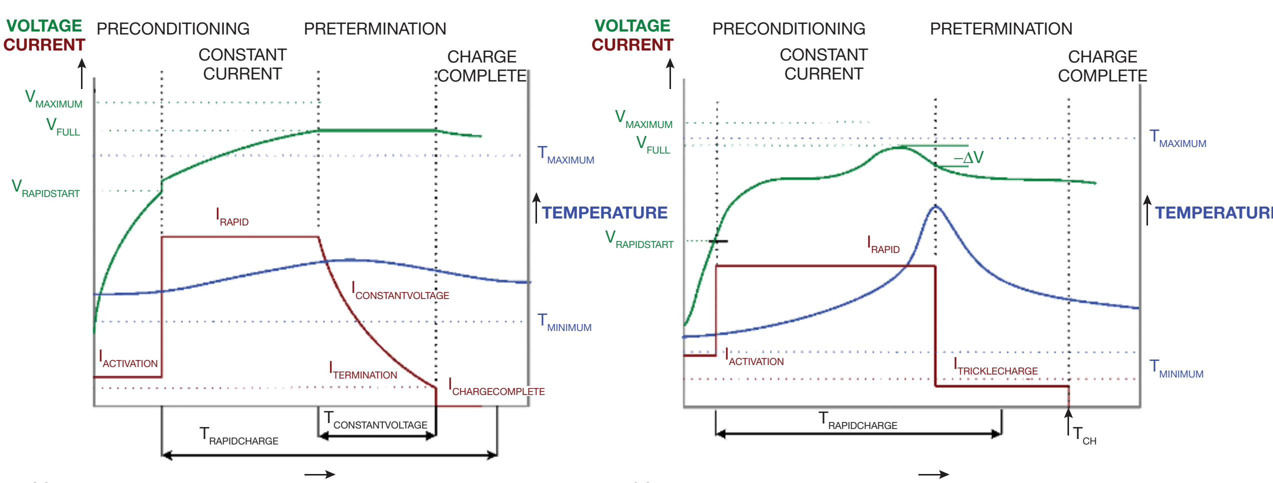


Figure 1 From the battery charger's perspective, the main difference between lithium-ion-battery chemistry (a) and NiMH-battery chemistry (b) is the charge profile.

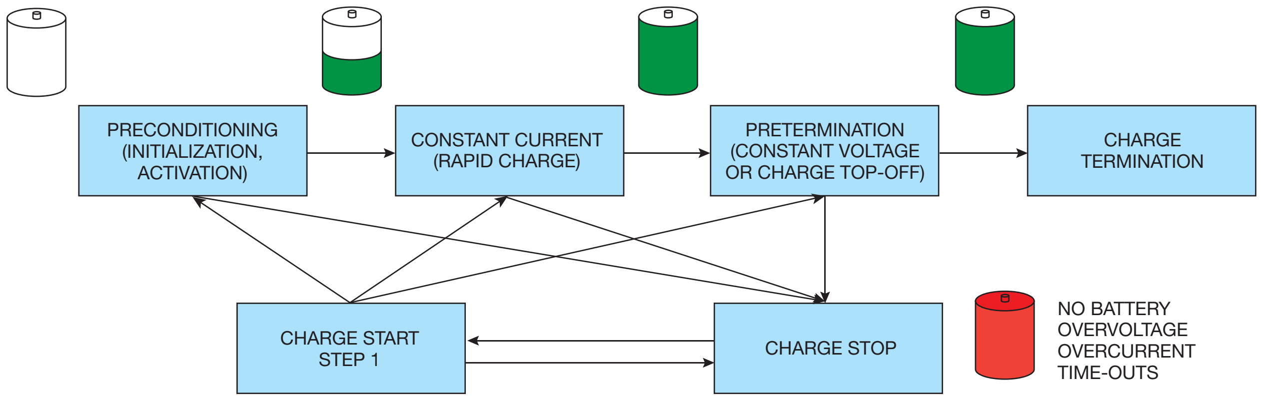


Figure 2 A state machine with predefined voltage, current, temperature, and time-out values can simplify the battery-charging profile for lithium-ion and NiMH batteries.

From the battery charger's perspective, the main difference between chemistries is the charge profile (**Figure 1** and **Reference 3**). Lithium-ion batteries use a constant-current, constant-voltage charge profile. If the battery voltage is lower than the constant-current threshold at start-up, the battery charger supplies a small amount of current—approximately 10% of the battery capacity. During this preconditioning stage, the battery's voltage gradually increases with the charge current. When the voltage reaches the rapid-charge threshold, the microcontroller increases the charge current to approximately 100% of capacity. This constant-current stage is maintained until the battery voltage reaches the specified voltage. The battery charger then enters the constant-voltage stage, during which the charge current decreases while the battery voltage remains at the specified voltage. When the current decreases until it reaches the termination current,

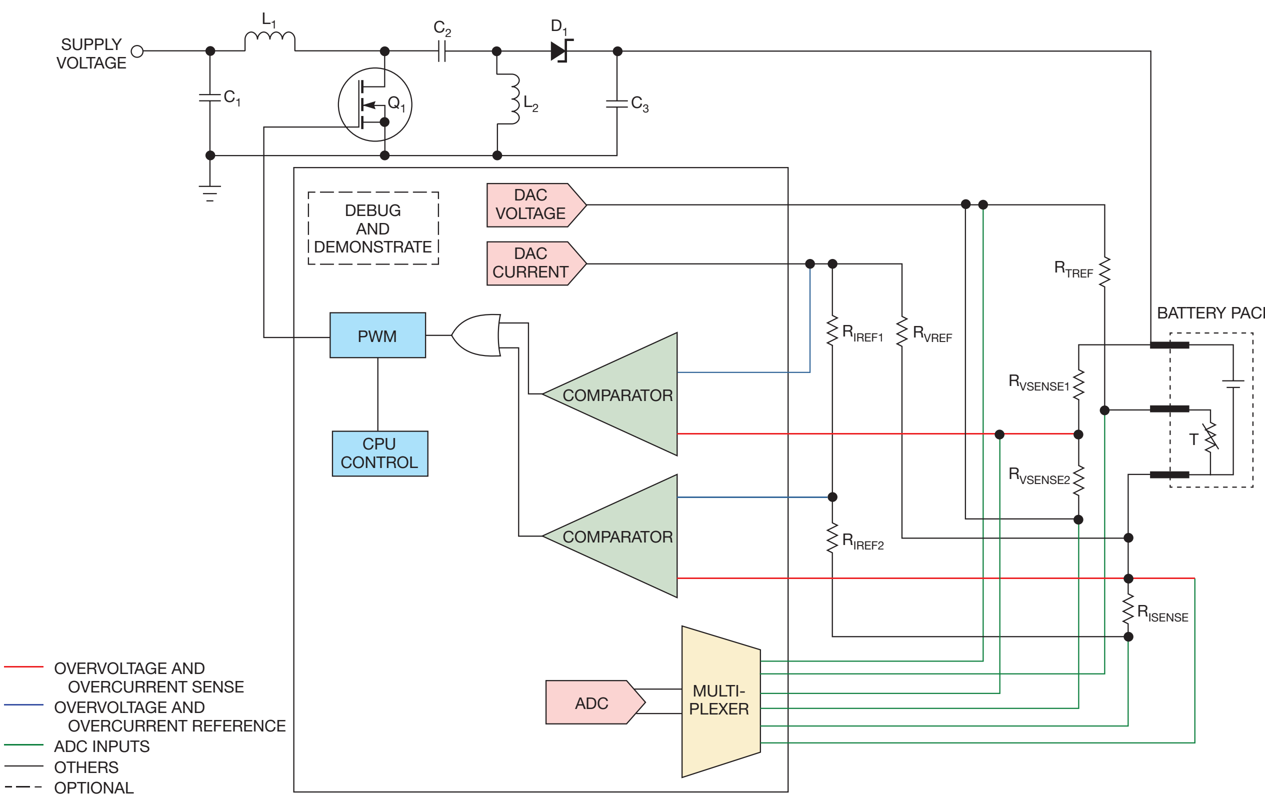


Figure 3 Depending on the battery chemistry you choose, the microcontroller goes through the state machine of the battery and controls the charge current. The external hardware for sensing and controlling battery charging is the same for both chemistries.

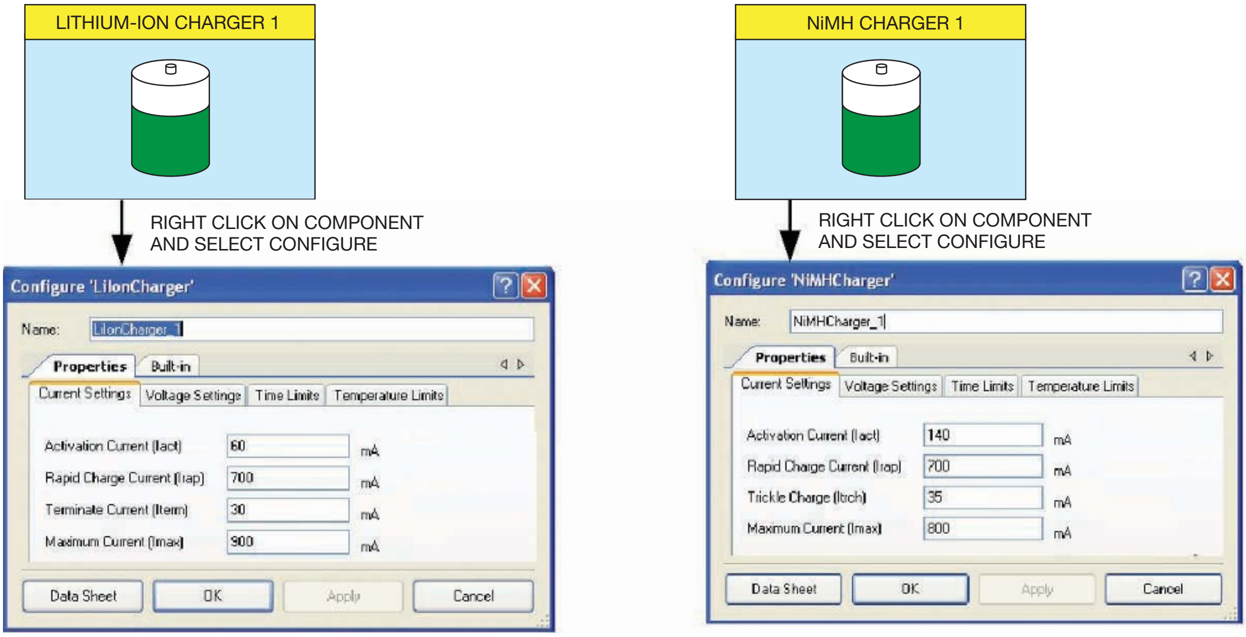


Figure 4 You use a graphical user interface to enter the parameter limits of battery chemistries.

the battery voltage remains the same, and battery charging terminates.

The current in the battery changes by a few degrees Celsius during charging. If any of the battery conditions—voltage, current, or temperature—are outside the specified range for the corresponding battery-charger stage, the battery charger shuts down the charging for protection.

The first two charger stages of an NiMH battery are similar to those of a lithium-ion battery: activation with 20% capacity and constant current with 100% capacity. A drop in the battery voltage and a drop in temperature indicate the end of the constant-current stage in NiMH batteries, whereas the current remains constant. After this decrease in voltage, the NiMH-charger profile enters a charge-top-off stage, during which the current decreases to a trickle level of approximately 5% of capacity. This stage provides a small amount of charge current for a constant amount of time before charge termination.

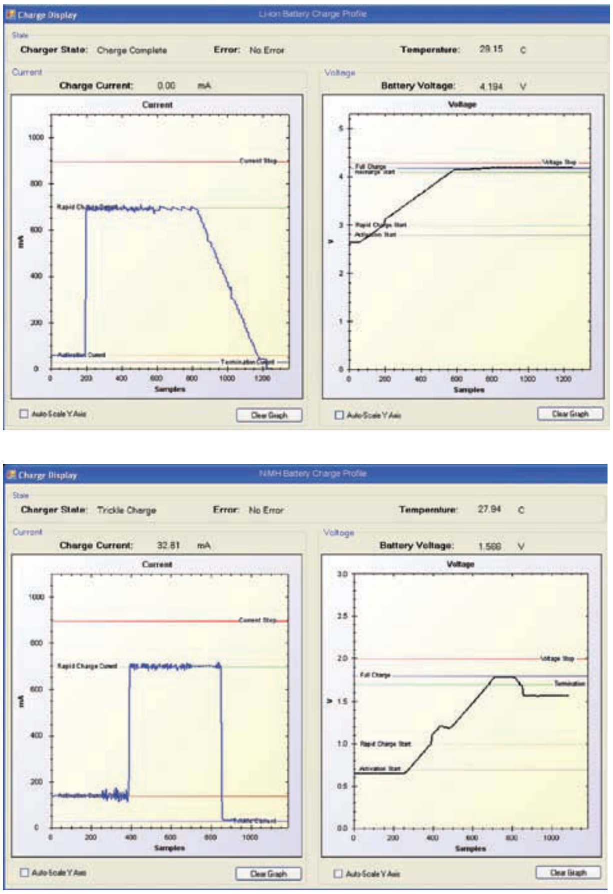
LISTING 1 PSEUDOCODE

```
#define LIIon 0
#define NIMH 1
#define BATTERY_PROFILE 0

void main()
{
Measure_Battery_Parameters(); //Use ADC to measure V, I and T
Get_Battery_State();
Control_PWM_DutyCycle();
}

Get_Battery_State()
{
          if(BATTERY_PROFILE == LIION)
          {
                    //set battery state for Li-Ion
          }
          else if(BATTERY_PROFILE == NIMH)
          {
                    //set battery state for NiMH
          }
          else
          {
                    //battery type error
          }
}
```

Using these charging requirements, you can simplify battery charging to different levels using a state machine with predefined voltage, current, temperature, and time-out values. The microcontroller's state machine controls the state of the battery and the amount of current required for battery charging. **Figure 2** shows a simplified state machine for charging both types of batteries.

Depending on the battery chemistry you choose, the microcontroller goes through the state machine of that battery and controls the charge current. The profile for charging a battery can be preprogramming, pre-start-up, or automatic decision. For the first two methods, the microcontroller derives the type of the battery from user input. In preprogramming, the module software chooses the type of battery charging, and the microcontroller is programmed with the required profile. This type of decision suits applications in which charging is an additional feature. In such applications, the battery type is known for a product.

In pre-start-up, the microcontroller uses a conditional check, which can be as simple as a switch position that the microcontroller checks during start-up, to determine both the battery profiles and the choice of profile. In automatic check, the microcontroller automatically makes this decision after start-up and chooses the battery-charger profile by detecting the type of battery. For example, a typical voltage range for a single-cell NiMH battery is 0.9 to 1.25V, whereas a lithium-ion cell's voltage ranges from 2.7 to 4.2V. Similarly, the temperature ranges also differ, and the microcontroller can save and compare these values during start-up. The automatic-check approach works only under certain condi-



(a)

(b)

Figure 5 A battery emulator emulates the lithium-ion (a) and NiMH batteries (b) to obtain the graphs in real time.

tions. In general, the preprogramming and preruntime decisions work in most applications. This article focuses on the preprogramming decisions for applications in which battery charging is an add-on feature.

Both chemistries use the same hardware for sensing and controlling the battery charger (**Figure 3**). To determine the battery's state voltage, current and temperature measurements are made by multiplexing these inputs to an ADC in the microcontroller. The firmware uses these values to determine the state, and changing the duty cycle of the PWM (pulse-width modulator) controls the charge current. The PWM's output connects to the gate of the MOSFET in the SEPIC that controls the current flowing into the battery. These steps involve the CPU and thus have some latency. Some batteries, including lithium-ion cells, are sensitive to overcharging and can become unstable at higher voltages. Comparators add hardware-protection circuits against overvoltage and overcurrent conditions. These comparators shut off charging until a user resets them, or until the battery reaches a safe condition.

Depending on the measured parameter values and the battery chemistry, the CPU determines the state of the battery and changes the duty cycle of the PWM accordingly. Traditionally, the conditions the CPU requires to detect the profile are constants in the code, and programmers manually change them (**Listing 1**).

When the profile requires modification, set the battery profile to zero or one to switch between the two profiles. The program saves the voltage, current, and temperature limits for all of the states as constants, and they change accordingly. If the same battery types require different voltage levels, you must change the code to enter the new parameters, meaning that the user of the application must be aware of the code to change the profiles and limits for battery charging. By taking a modular approach, you can enter parameters for changing the battery-charger profile when you select the appropriate IP (intellectual-property) blocks. **Figure 4** shows the module encapsulations for lithium-ion and NiMH batteries.

By using these modules, an application designer can add the charger module to an application and set up the appropriate profile. The module also generates all of the other hardware blocks, including the comparators and the PWM, and the software state machines. Using a reprogrammable architecture, such as Cypress Semiconductor's (www.cypress.com) PSoC (programmable system on chip), you can program and implement hardware modules with the software application. Developers used this method to program the hardware in **Figure 3** with NiMH-battery-charge profiles. Adding a USB (Universal Serial Bus) module to the product allows the developers to send the battery parameters to the computer. The data was plotted using a software tool in C#, although any other form of communication and a similar tool can be used to plot the data. A battery emulator was used to emulate the lithium-ion and NiMH batteries to obtain the graphs in real time (**Figure 5**).

The current has switching noise due to the change of voltage using a battery emulator. Because the voltage changes faster when using a battery emulator, the response and settling time of the PWM output in response to a change in voltage is seen as switching noise. The change of voltage in a battery is gradual, and switching noise is thus insignificant with a real battery.

With a simple change in the firmware of an SOC (system on chip), you can develop a multichemistry-battery charger with the same hardware. Making modules of the profiles in components facilitates battery charging as an added feature to a main application.EDN

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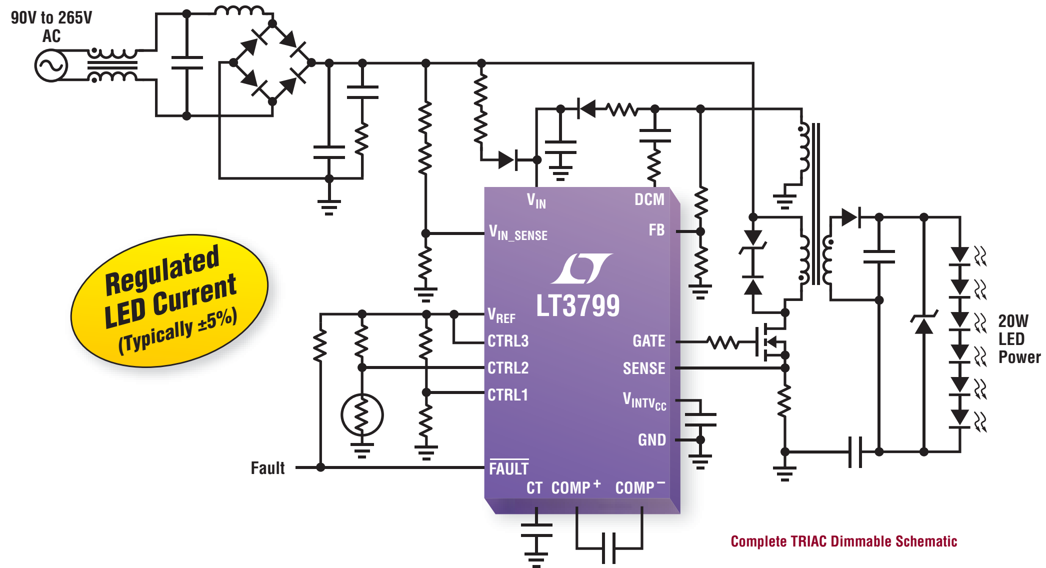
AUTHOR'S BIOGRAPHY

Archana Yarlagadda is a senior applications engineer at Cypress Semiconductor, focusing on PSoC applications, analog- and mixed-signal designs, and the development of analog sensor interfaces with PSoC. She has a master's degree in electrical engineering from the University of Tennessee (Knoxville, TN).

Isolated LED Current Control with Active PFC

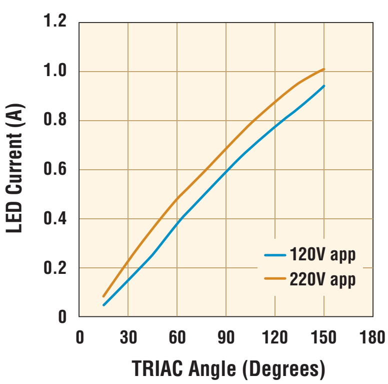


Complete TRIAC Dimmable Schematic

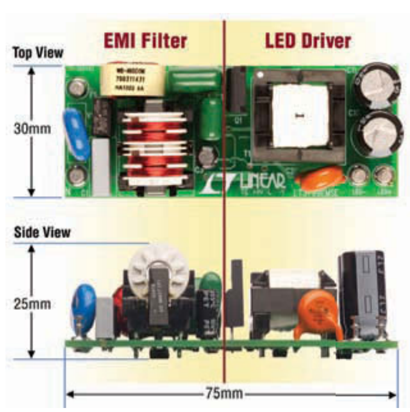
TRIAC Dimmable LED Driver Needs No Opto-coupler

Our LT®3799 isolated LED controller with active power factor correction (PFC) is specifically designed for driving LEDs over a wide input range of 24V to 480V+. It is ideal for LED applications requiring 4W to over 100W of LED power and is compatible with standard TRIAC in-wall dimmers. The LT3799's unique current sensing scheme delivers a well regulated current to the secondary side with no opto-coupler, enabling it to provide ±5% LED current accuracy. It also offers low harmonic distortion while delivering efficiencies as high as 90%. Open and short LED protection ensures long term reliability and a simple, compact solution footprint addresses a wide range of applications.

LED Current vs TRIAC Angle



LT3799 Demo Board (25W)



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LINEAR TECHNOLOGY

Compensate for four-wire sensor errors

Septimiu Pop and Ioan Ciascai,
Technical University of Cluj Napoca, Cluj Napoca, Romania

Resistive pressure sensors that use two resistive elements and four wires are useful in pressure-monitoring applications. When the pressure rises, one resistance rises and the other falls. Accurate measurements with resistive sensors require compensation for losses due to wire resistance, especially when wire lengths are tens of meters. The compensation method in this Design Idea relies on the equal resistance of wires: $R_{L1}=R_{L2}=R_{L3}=R_{L4}=R_L$ (**Figure 1**).

A microcontroller or computer can calculate the resistance of the sensors using a differential voltage across sensor elements R_{S1} and R_{S2}. Resistances R_A, R_{REF}, and R_B and the sensor resistance limit the current through R_{S1} and R_{S2}. To measure the sensor values, the circuit uses an Analog Devices (www.analog.com) AD7705 ADC, which has three pseudodifferential inputs that provide 16-bit resolution. In this application, the AD7705 operates in buffered mode—that is, the input bias current is less than 1 nA. In buffered mode, the analog inputs can handle large source impedances, but the absolute input voltage must be from ground plus 50 mV to the drain-to-drain voltage minus 1.5V. Resistance R_B provides an input common voltage.

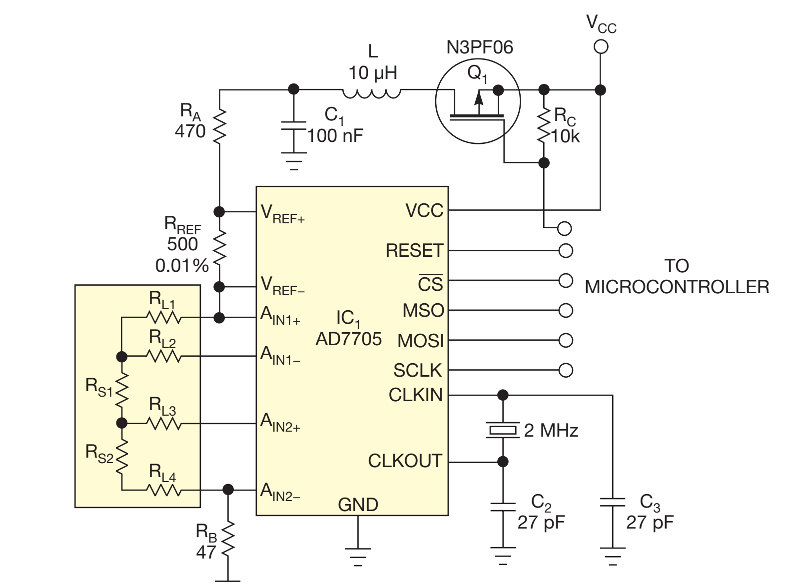

Figure 1 A measurement circuit measures the values at three points, and a microcontroller can calculate the sensor values.

The measurements depend on the value of reference resistor R_{REF}. For best accuracy, R_{REF} must have a tolerance of 0.01% and must have a low temperature coefficient. To avoid sensor self-heating, you should pulse the excitation current; software through Q_1 controls the pulse width.

The AD7705 performs the data acquisition through three channels. The sensors connect directly to the AD7705's input channels, which make three successive acquisitions. Because the excitation current is the same in all sensor elements, the software computes each input voltage for the sensor elements in the following sequence:

1. A_{IN1+}, A_{IN1-} compute R_L;
2. A_{IN2+}, A_{IN2-} compute $R_{S2}+R_L$;
3. A_{IN1-}, A_{IN2-} compute $R_{S1}+R_{S2}+R_L$.

You can compute the resistances R_{S1} and R_{S2} by subtraction. The AD7705 has a PGA (programmable-gain amplifier) that amplifies low input signals. The part contains self-calibration and system-calibration options that eliminate gain and offset errors in the part or in the system.

The pressure measurement also depends on both the resistance ratio and the temperature through the **equation** $P=F(R_{S1}/R_{S2},T)$. The parameter T is a compensation factor for the resistive sensors' temperature dependence, $T=F(R_{S1}+R_{S2})$. EDN

LED-current limiter accepts ac or dc

Roger Griswold, Micrel, San Jose, CA

LED drivers have lots of features and require plenty of external components. When your application requires no PWM (pulse-width-modulated) dimming or controlled frequency operation, your primary concern may be that too much current could damage or destroy your LEDs. In this case, you can make a simple LED-current limiter from a common low-dropout linear regulator. The circuit in **Figure 1** is an LED light bulb for a landscape-lighting system. Landscape lighting typically operates from 12V ac, and peak voltage is approximately 17V. Because the regulator is in series with the LED string, the LED-string current equals the regulator's output current.

The circuit uses reasonably priced, 150-mA, warm-white LEDs; low-cost rectifier diodes; and Micrel's (www.micrel.com) 2.5V MIC5209-2.5YS regulator (**Figure 1**). The regulator must source at least the required LED current and handle the peak input voltage minus the drop across two of the four rectifier diodes and the drop across the LEDs. Selecting a regulator with the lowest possible output and dropout voltages lets LED current flow for a larger portion of each ac cycle, and it reduces the power requirement of current-setting resistor R_1. As output and dropout voltages decrease, cost increases. The regulator sees the peak voltage at approximately 5.1V and dissipates approximately 0.2W.

The MIC5209-2.5YS' output voltage regulates to 2.5V between its output and ground. R_1 sets the LED-string current using $R_1=(2.5/I_{LED})$, where I_{LED} is the LED-string current. With a value of 16.9Ω for R_1, the string current is 148 mA. The circuit has slightly more than 2.5W peak dissipation. With an ac input, the current flows only about half the time, so the average power dissipation is approximately 1.26W.

You can easily modify the circuit to accept almost any input voltage. Simply change the number of LEDs and make sure that the rectifier diodes can handle the reverse voltage. Add or subtract one LED for each 3.33V increase or decrease in peak input voltage. Don't use LEDs for the rectifier diodes to get more light output because LEDs don't have sufficient reverse-breakdown voltage and will fail. The input bridge accepts either ac or dc and negates the need to worry about the polarity of a dc input. EDN

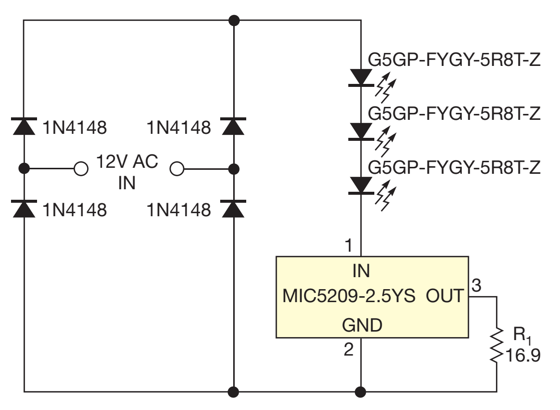

Figure 1 A low-cost regulator is the heart of an LED-current limiter.

Voltage inverter employs PWM

Jeff Wilson, STMicroelectronics, Schaumburg, IL

This Design Idea describes a circuit employing a small microcontroller-based sensor module with only three connections: 5V dc, an RS-232 transmit-data output, and ground. A dedicated single-voltage level shifter or a dc/dc converter would be too costly, but the design still needs to supply ±3V at 1 mA to drive the transmit-data pin. Because a spare PWM (pulse-width-modulator) output on the 5V microcontroller could drive ±5 mA at nearly 5V, a PWM-based voltage inverter using a BAT54S dual-series Schottky diode, two capacitors, and a limiting resistor would produce the negative voltage (**Figure 1**).

The microcontroller's PWM output drives the inverter with a 1-kHz, 50%-duty-cycle, 0 to 5V waveform. When the PWM output is 5V, it charges C_1. The lower diode in D_1 biases in a forward mode to connect the terminal to ground. When the PWM output is low, it transfers the charge in C_1 to C_2 by forward-biasing the upper diode in D_1. Meanwhile, it inverts the charge by taking the positively charged terminal of C_1 nearly to ground potential. When the PWM output switches high again, the cycle repeats.

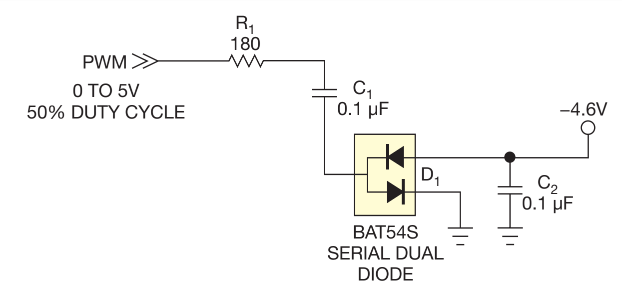

Figure 1 The diodes and capacitors produce a negative voltage.

Due to D_1's minimum voltage drop of 0.2V, it is impossible to get to −5V from 5V, so the voltage output will be approximately −4.6V, with 0.2V loss in each phase. The design requires a limiting resistor,

R_1, only when the driving microcontroller is sensitive to the current transients when switching or if the switching transients disturb the analog inputs on the microcontroller.

The PWM's timebase is 1 kHz, so component values must accommodate that frequency. If you need other frequencies, you must calculate new component values using the following **equation**: C=1/(10×F×R), where C is the value of C_1 and C_2, F is the PWM switching frequency in hertz, and R is the total resistance of the PWM's output-driving circuit.

When calculating the total resistance of the PWM output, you must take into account the drive rating of the digital output. A simple substitution for the value of R is V/A, where V is the drive voltage of the PWM's output and A is the current drive of the output in amps. For example, the original values for this design are R=V/A=5V/0.005A=1000Ω, and C=1/(10×F×R)=1/(10×1000 Hz×1000Ω)=1×10^{-7}, or 0.1 μF.

You can also use this circuit as a negative-voltage supply for ADC/DAC and op-amp dual supplies. For analog usage, you probably need to use additional filtering or micropower voltage regulators on the output to filter out the switching transients. EDN

Form positive pulses from negative pulses

Vladimir Rentyuk, Zaporozhye, Ukraine

The circuit in this Design Idea converts negative pulses to positive pulses. Although that task may seem simple, the negative pulses have amplitudes of –5 to –2V. The positive pulses also need different pulse widths, depending on the application, and the negative pulses are trapezoidal. The pulses must travel over a long-distance transmission line to a control device. Several circuits solve the problem, depending on the amplitude and shape of the pulses.

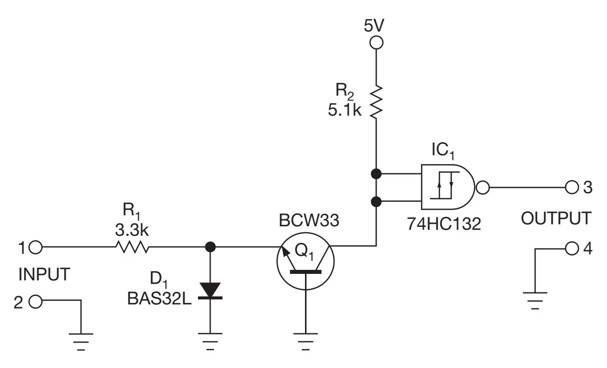

Figure 1 This circuit uses a single power supply and has good noise immunity but doesn't reliably convert pulses of trapezoidal shape.

Figure 1 shows a circuit that needs just one 5V power supply. Its high trigger threshold maximizes noise immunity. This circuit requires a high input current that's comparable to a collector current. It also needs a CMOS or TTL (transistor-transistor-logic) inverter to trigger on a threshold voltage. If the input pulse is a trapezoid, the output pulse width doesn't correspond to the input pulse widths. You can calculate a threshold, V_{T-}, as $V_{T-}=-[(V_+-V_{IH})\times R_1/R_2+0.62]$, where V_{T-} is the lower voltage threshold, V_+ is the power-supply voltage, and V_{IH} is the high-level input voltage of the 74HC132. **Figure 2** shows the input and output waveshapes.

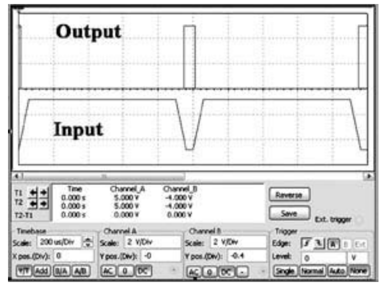

Figure 2 Output pulses are approximately the width of the most negative part of the input.

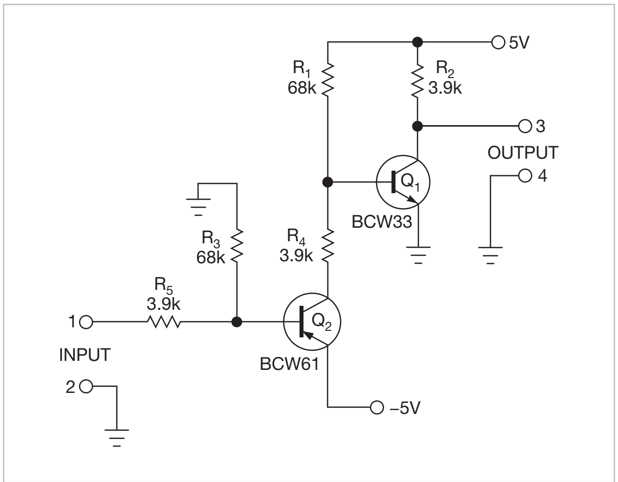

Figure 3 You can use this circuit to convert pulse polarity, but it needs two power supplies.

Figure 3 shows a pulse shaper that can convert 3-μsec negative-polarity pulses to positive pulses. The output pulse's width is sufficiently close to the pulse width of the input pulse. This circuit requires neither high input current nor an inverter. It has a lower voltage threshold than the circuit in **Figure 1**: $V_{T-}\geq-0.3V$, but the circuit in **Figure 3** needs two supply voltages: ±5V. **Figure 4** shows the waveforms for the circuit in **Figure 3**.

The circuit in **Figure 5** goes a step further. It uses an inexpensive LM211 or LM311 IC comparator and produces positive output pulses that fully correspond to the pulse width of the input pulse on its adjusted level (**Reference**

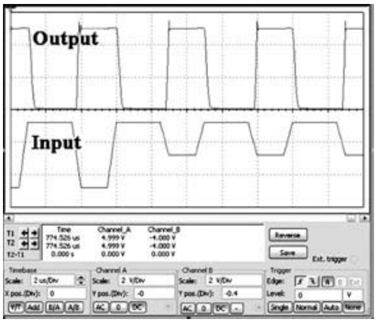

Figure 4 Pulse widths are a minimum of 3 μsec.

1). Resistors R_3 and R_4 set the comparator's threshold voltage, but it depends on the value of the negative supply's voltage. You can calculate the threshold voltage using the **equation** $V_{T-}=[V_-/(R_2+R_4)]\times R_4$, where V_- is the negative power-supply voltage. **Figure 6** shows the circuit's waveforms.

You can use the less expensive LM211 comparator if the pulse width is 2 μsec or longer. Otherwise, use a high-speed comparator. Doing so eliminates the need for the additional output resistor, R_1. The LM211 requires this resistor because of the IC's open-collector circuit. This circuit needs two supply voltages.

The circuit in **Figure 7** can convert negative-polarity pulses to positive pulses where the output does not depend on the amplitude of input pulses. This version uses a single supply and a 555 timer (**Reference 2**). It produces output pulses of positive polarity with a desired pulse width. Resistors R_1 and R_3 establish a threshold of actuation. You can calculate this threshold using $V_{T-}=V_+/3\times(1-2R_3/R_1)$, where V_+ is the 555's power-supply voltage. Resistor R_2 and capacitor C_1 set the pulse width. The **equation** $t=1.1R_2C_2$ calculates the duration of the output high state. For proper operation of the circuit, the actuation pulse must be shorter than the desired pulse width, and the pulse period must be greater than t. Resistor R_3 must have a value of at least 1.5 kΩ. Resistor R_4 is optional.

In contrast to the circuits in **figures 1**, **3**, and **5**, the circuit in **Figure 7** operates on low-resistance loads, with output source or sink current as high as 200 mA, or a high-capacity load. The circuit requires no additional inverter or driver. Resistor R_5 protects the IC from short circuits at its output. **Figure 8** shows the circuit's waveforms. EDN

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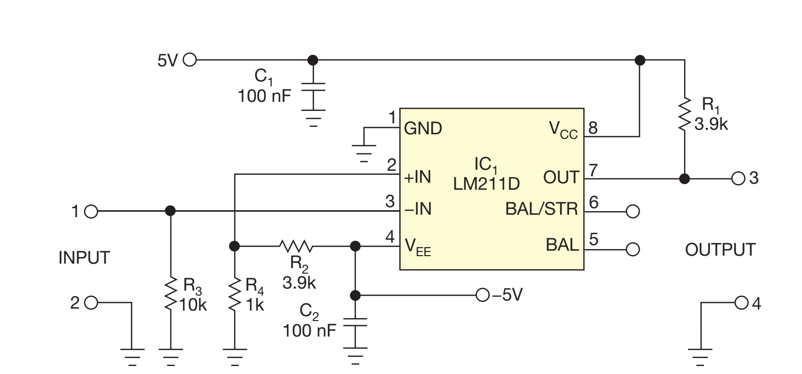

Figure 5 A comparator in this circuit produces accurate pulse widths.

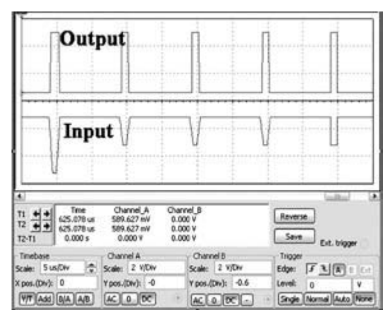

Figure 6 Positive output pulses are nearly the same width as negative input pulses.

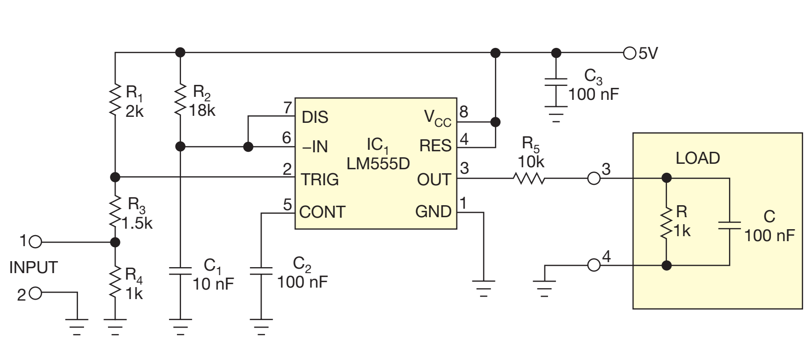

Figure 7 This pulse converter uses a 555 timer.

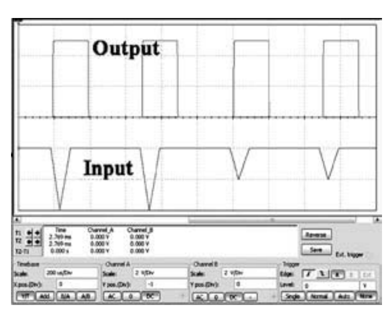

Figure 8 The 555 timer in Figure 7 produces positive pulses of the desired width.

India's ROHS turns up the heat

The EU's (European Union's) version of the ROHS (restriction-of-hazardous-substances) directive seems to be approaching clarity, but India's version of ROHS appears to be as clear as mud. The EU has officially adopted a revised ROHS, which clarifies a number of issues pertaining to the measure and bans six substances from electronics products sold in Europe.

Under the original version, the scope of products that had to comply with ROHS left a lot of room for interpretation. The revision tightens those loopholes. Additionally, the EU revision specifies that cables and various attachments to electrical and electronics equipment must also comply with the law, which bans substances such as lead, mercury, and cadmium from electronics products for sale in the EU.

India's version, which is moving closer toward its May 2012 implementation, limits the use of 20 substances from electronics products for sale in India. Global distributor element14, which provides updates and analysis of global environmental legislation, has posted a summary of India's ROHS on its Web site (http://bit.ly/muZp7Q). According to element14, the proposals on the disposal of WEEE (waste electrical and electronic equipment) do not say whether these substances are restricted or that manufacturers should attempt to avoid them; do not state whether the threshold values refer to the concentrations in the finished product, in homogeneous materials, or in something else; provide no exemptions or any mechanism for requesting exemptions; and lack clarity of limits.

Inconsistencies among global environmental laws are ongoing concerns in the electronics industry, which must greatly modify processes and materials to meet ROHS requirements. The ban of lead from solders in manufacturing has been particularly irksome because unleaded substitutes have worse performance than do leaded substances.

The element14 proposal also notes the next set of challenges, including a requirement that medical equipment adhere to the ban, whereas the EU version currently does not. India's ROHS also bans substances, including some flame retardants, that have no viable alternatives.

Similar to the EU legislation, India will require manufacturers and importers to supply only ROHS-compliant products and to provide written documentation supporting compliance. This struggle has been ongoing in the electronics supply chain because documenting compliance often requires the disclosure of information that component makers regard as proprietary.

IMAGE: THINKSTOCK

There's no question that electronics manufacturers will adhere to these measures. The industry has, with some difficulty, complied with the EU's ROHS. In the past two years, China has passed its version of ROHS, and India now also has. The European Union is an important but relatively small market for electronics manufacturers. China and India, on the other hand, are the two largest markets for electronics products. Electronics manufacturers need to come up with new ways to build their products and keep users safe; otherwise, the race is on to develop new flame retardants.

—by Barbara Jorgensen, EBN Community Editor

This story was originally posted by EBN: http://bit.ly/jKIYH8.

OUTLOOK

APPLE SPENT $17.5 BILLION ON CHIPS IN 2010

Apple Inc (www.apple.com) has become the leading buyer of semiconductors among OEMs, according to IHS iSuppli (www.isuppli.com). Thanks in large part to demand for its iPad tablet and iPhone smartphone, Apple in 2010 bought $17.5 billion worth of semiconductors, a 79.6% increase from $9.7 billion in 2009.

IHS iSuppli notes that Apple is likely to continue increasing its semiconductor spending during the coming years at an above-average pace in 2011 and beyond. The market-research company expects Apple's semiconductor spending to exceed that of Hewlett-Packard (www.hp.com) by $7.5 billion in 2011, up from $2.4 billion in 2010, for a total of $22.4 billion that Apple will spend this year on semiconductors.

The spending illustrates consumer trends toward mobility. IHS iSuppli reports that Apple, which has heavily bet on mobility, spent approximately 61% of its semiconductor budget in 2010 on wireless products, such as iPhones and iPads. According to IHS iSuppli data, Apple placed its bets wisely. Smartphone shipments in 2010 rose 62%, and tablet shipments were up by more than 900%.

—by Suzanne Deffree

OPTOELECTRONICS AND DISPLAYS

2A, single-inductor RGB-LED driver targets use in portable projectors

The 2A LM3435 driver for portable projectors sequentially drives three common-anode high-brightness RGB LEDs with one inductor. The device includes an I^2C control interface for LED-current control. Other portable- or pocket-projector LED designs require a separate driver for each red, green, and blue LED, and each circuit requires an inductor. Such designs are bulky and costly, comprising multiple components to accurately drive the LEDs. These projectors are often smaller than a 2.5-in. hard drive, posing space constraints. By sequentially driving three RGB LEDs at 60 Hz or higher speeds, the LM3435 matches the operation requirements of liquid-crystal-on-silicone or digital-light-processing devices and requires only one inductor and a few passive components. The LM3435 sells for $4.50 (1000).

National Semiconductor, www.national.com

Integrated LED driver aims at LCD-backlighting displays

The UBA3077 for use in backlighting LCDs has 94% efficiency, enabling designers to engineer thinner LCD panels with less power consumption and heat dissipation. The UBA3077 comprises three independent channels, each with its own integrated boost converter and current source, making the application's design immune to extra heat dissipation due to voltage mismatch in the LED strings. The device features integrated MOSFETs for boost converters and current sources and has individual PWM controls for each channel. Operating with a supply of 10 to 42V, the UBA3077 can drive as many as three strings of 20 LEDs, each rated as high as 150 mA. The device sells for $3.20 (1000).

NXP Semiconductors, www.nxp.com

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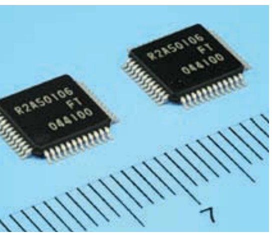
LED-driver IC for back-lit LED TVs has low power consumption

The R2A50106FT LED-driver IC for LED backlights has 20% lower power consumption than other units. The device has eight constant-current-driver channels that can drive high-luminosity LEDs, reducing the need for external components and easing the design of high-luminosity-LED-backlight systems. Optimal voltage depends on factors such as the LED, or forward voltage, and the output volume, or number of elements that connect in series. On-chip protection functions include the ability to detect open or shorted LEDs row by row; when a fault occurs, the driver stops operation of only the affected row. The R2A50106FT sells for $2 (one).



Renesas Electronics, http://am.renesas.com

LED-backlight driver suits medium and large displays

The multioutput A8516 white-LED/RGB driver for backlighting LCD monitors and TVs integrates a boost controller to drive an external MOSFET. It also includes six internal current-sink channels that can sink as much as 80 mA each, and designers can combine channels to achieve even higher currents. The boost converter operates in programmable constant-frequency current-mode control. An external resistor sets the LED sink current, and PWM dimming allows the control of LED currents. The A8516 protects against overvoltage, open or shorted LED strings, and overtemperature. A dual-level, cycle-by-cycle current-limit function provides soft start and protects against overloads. The device sells for $1.54 (1000).

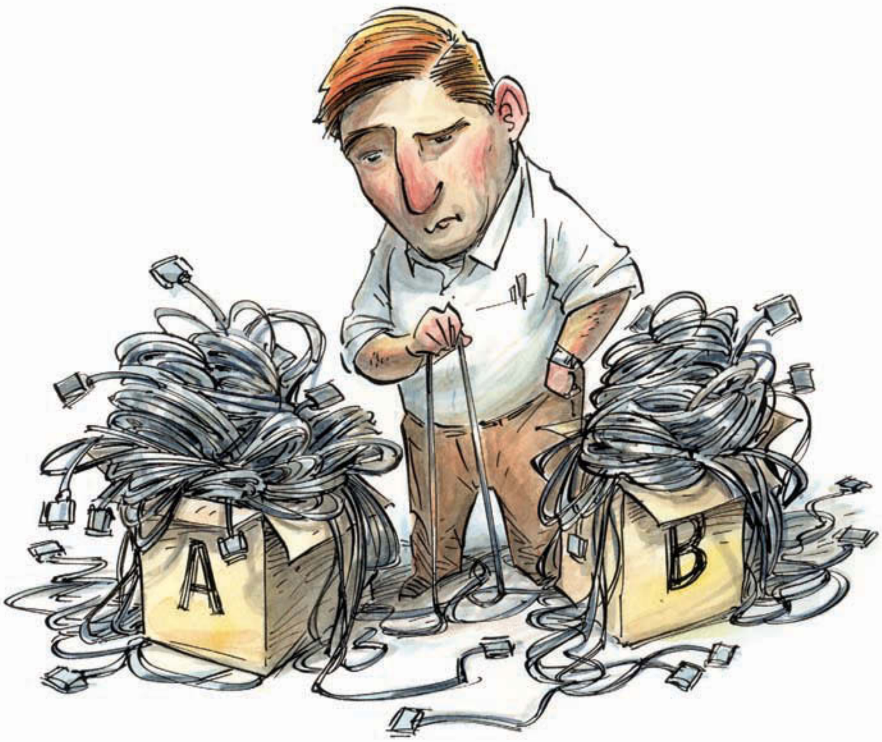
Allegro Microsystems, www.allegromicro.com

Hot-tested LED requires no binning

Hot-tested and specified at a junction temperature of 85°C, the Luxeon A LED ensures real-world operating-condition performance and simplifies the design process. The LED needs no binning, typically a burden on luminaire manufacturers. All Luxeon A emitters fall within a single three-step MacAdam Ellipse at 2700 and 3000K and deliver superior quality of light with color consistency from unit to unit. Prices start at $4.44 (one).

Philips Lumileds, www.philipslumileds.com

Unable cable proves stable



It was another quiet day in my department, component engineering, which was responsible for ensuring the quality of vendor-supplied components. The peace ended when a call came from manufacturing, informing us that the production line had stopped due to a failing communications cable. The shift manager explained that the manufacturing department had exhausted its stock of working, 50-foot RS-232 cables, which our company had procured from two vendors. During final testing of the entire machine, cables from Vendor A usually failed, but cables from Vendor B always worked fine. When a cable failed, workers tossed it into a nearby box but did not discard it. Finally, manufacturing had exhausted its supply of cables from Vendor B and had no more working cables from Vendor A.

At the time, I was unaware that, before I joined the department, manufacturing had submitted Vendor A's cables to testing to find out why they had failed. I reviewed the filed test report and found that the extensively tested cables not only met but exceeded specifications. I retested a few samples from each vendor and found that Vendor A's cables in fact met and even exceeded specifications. I went to the production line and asked operators to run the final test run using a previously failing cable from Vendor A. The test program failed at one step. To understand what that step was, I reviewed the code for the test program. It was, however, in a language unfamiliar to me. So I asked to talk to the program's author. I then learned that the program's author was unavailable because the product had come from another—now shuttered—manufacturing location. Test code and test fixtures had come from this remote manufacturing plant. After seeking help with deciphering the code and noting that test fixtures included a "wrap-back" plug for the remote end of the RS-232 cable, I found the problem: At the failing step, the test program activated a DTR (data-terminal-ready) signal and then tested to verify that a DSR (data-set-ready) signal activated as a response. Because the test did not include an external modem, it relied on a jumper wire in the wrap-back plug between DTR and DSR. The wrap-back plug simulated the presence of a modem.

CABLES THAT WE CONSIDERED GOOD WERE INFERIOR IN THAT THEY HAD SUFFICIENT CROSSTALK BETWEEN DTR AND DSR SIGNALS TO FOOL THE TEST PROGRAM.

For those of you who have long since forgotten RS-232 standards, this handshake sequence was the normal one between a machine and a modem. Inspection of the wrap-back plug showed a missing jumper between DTR and DSR. The obvious question then was how either vendor's cable could pass the test. Further experiments showed that crosstalk from DTR to DSR with Vendor B's cables was so large that even without a jumper in the wrap-back plug, enough signal was returning on DSR through crosstalk that the test could assume that the machine was OK. Vendor A's well-made cable had low crosstalk, causing the test's failure. Cables that we considered good were inferior in that they had sufficient crosstalk between DTR and DSR signals to fool the test program. By installing the missing jumper in the wrap-back plug, all those assumed bad cables from Vendor A suddenly allowed production to resume. Luckily, production had saved them so long that there was a large stock on hand. EDN

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DANIEL VASCONCELLOS